Image Correction ICs

Image Correction IC for Panel

BU1523KV

No.11060EAT05

●Description

BU1523KV is an image quality adjustment IC for in-vehicle displays. It can control brightness, contrast, hue, intensity, sharpness, etc. It is equipped with both RGB and YCbCr as input/output interfaces. It also incorporates LVDS output capability with an embedded LVDS transmitter.

●Features

1) RGB input data format
   Width of data bus 24bit
   Vertical/horizontal synchronizing and data enable signal
2) RGB output data format
   It is the same as the entry format
3) YCbCr input data format
   ITU-R BT.656-4 or synchronization signal YCbCr
   Width of data bus 8bit
   Vertical/horizontal synchronizing and data field signal
   Date range conform ITU-R BT.601 or full range
4) YCbCr output data format
   The same as the entry format
   Capable of processing BT.656 input to generate and output synchronization signal from SAV/EAV
5) RGB IF Image quality adjustment
   Contrast, Brightness, Hue, Chroma and Sharpness
   Independent RGB gamma correction
6) YCbCr Image quality adjustment
   Contrast, Brightness, Hue, Chroma and Sharpness
7) LVDS Transmitter
   Built-in LVDS transmitter
   Converts RGB24 bit, vertical/horizontal synchronization signal and data enable inputs into 4ch LVDS data streams
8) 2-line serial interface slave function
   The register in BU1523KV can be set
9) Package
   VQFP100

●Applications

In-vehicle display etc.

●Absolute maximum ratings

[Table 1]

Parameter	Symbol	Ratings	Unit
Supply voltage 1	VDDIO	-0.3～+4.0	V
Supply voltage 2	VDDI2C	-0.3～+4.0	V
Supply voltage 3	PVDD	-0.3～+4.0	V
Supply voltage 4	LVDD	-0.3～+4.0	V
Supply voltage 5	VDD	-0.3～+2.1	V
Input voltage range	VIN	-0.3～IO_LVL+0.3 *1	V
Storage temperature range	Tstg	-40～+125	℃
Power dissipation	PD	1000 *2, 1499 *3	mW

*1 IO_LVL is a generic name of VDDIO, VDDI2C
*2 IC only. In the case exceeding 25℃, 10mW should be reduced at the rating 1℃.
*3 When packaging a glass epoxy board of 70x70x1.6mm. If exceeding 25℃, 14.99mW should be reduced at the rating 1℃
* Has not been designed to withstand radiation.
* Operation is not guaranteed at absolute maximum ratings.

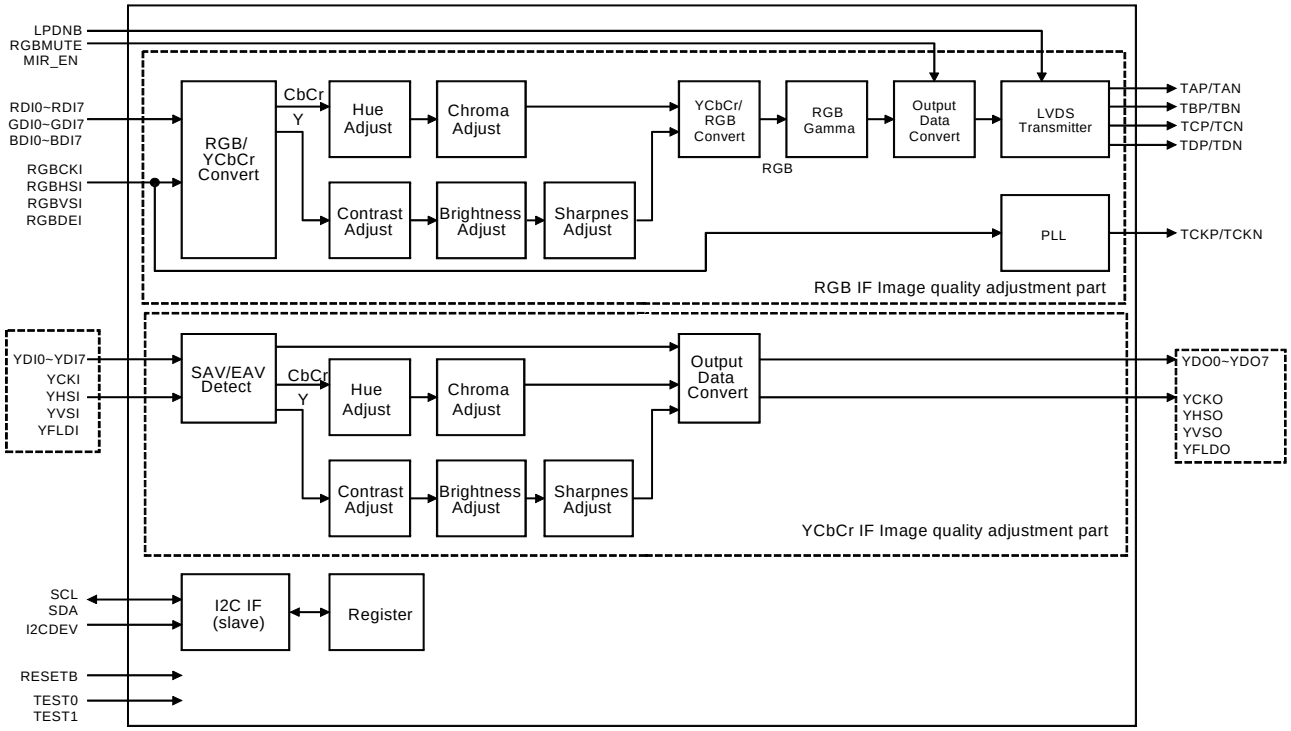
●Operating conditions

[Table 2]

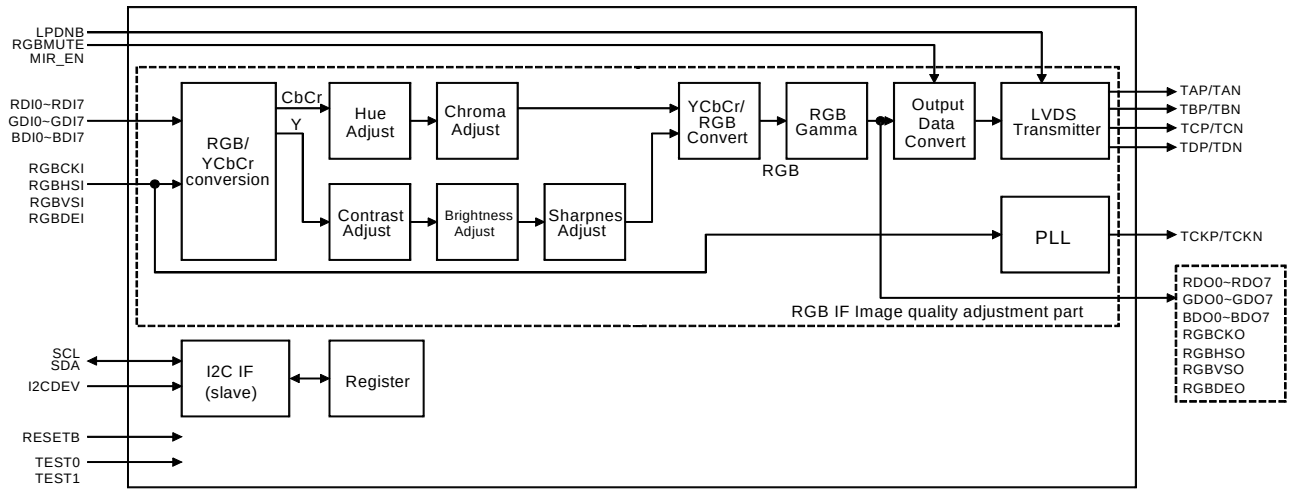
Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Supply voltage1(IO)	VDDIO	3.0	3.3	3.6	V
Supply voltage2(IO)	VDDI2C	3.0	3.3	3.6	V
Supply voltage3(PLL)	PVDD	3.0	3.3	3.6	V
Supply voltage4(LVDS)	LVDD	3.0	3.3	3.6	V
Supply voltage5(CORE)	VDD	1.65	1.8	1.95	V
Input voltage range	VIN	0.0	-	IO_LVL *1	V
Operating temperature range	Topr	-40	-	+85	℃

*1 IO_LVL is a generic name of VDDIO, VDDI2C.
* Please supply power source in order of VDD→ (VDDIO, VDDI2C, PVDD,LVDD).

●Block Diagram



The LVDS data output mode



The RGB data output mode (YCbCr interface cannot be used.)

Terminal selection from register

*Change their modes with register setting.

Fig. 1 Block diagram

●Terminal Functions・Equivalent circuit diagram

[Table 3 Terminal Functions (1/4)]

PIN No.	PIN Name	In/Out (*1)	Init (*2)	Function Description	PowerSupply System (*4)	I/O Type
1	BDI4	I	-	RGB B Data [4] input	a	A
2	BDI5	I	-	RGB B Data [5] input	a	A
3	BDI6	I	-	RGB B Data [6] input	a	A
4	BDI7	I	-	RGB B Data [7] input	a	A
5	RGBHSI	I	-	RGB H Sync input	a	A
6	RGBVSI	I	-	RGB V Sync input	a	A
7	RGBDEI	I	-	RGB Data Enable input	a	A
8	GND	G	-	Ground	a,b	-
9	RGBCKI	I	-	RGB Clock input	a	B
10	VDDIO	P	-	IO power source	a	-
11	I2CVDD	P	-	2-line serial interface IO power source	b	-
12	SDA	I/O	In	2-line serial interface data input / output (*6)	b	G
13	SCL	I	-	2-line serial interface clock input	b	H
14	GND	G	-	Ground	a,b	-
15	VDDIO	P	-	IO power source	a	-
16	VDD	P	-	CORE power source	-	-
17	YDO7/RGBDEO	O	Low	BT601 YcbCr data [7] / RGB data output	a	D
18	YDO6/RGBVSO	O	Low	BT601 YcbCr data [6] / RGB V Sync output	a	D
19	YDO5/RGBHSO	O	Low	BT601 YcbCr data [5] / RGB H Sync output	a	D
20	YDO4/BDO7	O	Low	BT601 YcbCr data [4] / RGB B data [7] output	a	D
21	YDO3/BDO6	O	Low	BT601 YcbCr data [3] / RGB B data [6] output	a	D
22	YDO2/BDO5	O	Low	BT601 YcbCr data [2] / RGB B data [5] output	a	D
23	YDO1/BDO4	O	Low	BT601 YcbCr data [1] / RGB B data [4] output	a	D
24	YDO0/BDO3	O	Low	BT601 YcbCr data [0] / RGB B data [3] output	a	D
25	YFLDO/BDO2	O	Low	BT601 Field output / RGB B data [2] output	a	D

* Fix an unused input pin to GND or VDDIO (Fix SDA and SCL to I2CVDD. TEST0 and TEST1 are excluded.) .

*1) “I” shows the input, “O” shows the output, “I/O” shows the bidirection, “P” shows the power supply, and “G” shows GND.

*2) “PD” shows the pull-down, “In” shows the input mode, and “Low” shows the Low level output.

*4) "a" in the column in the power supply system shows VDDIO, "b" shows I2CVDD, "c" shows LVDD, and "d" shows PVDD.

*6) “SDA” is output at "L" level when usually using it or is in the state of high impedance, and "H" level is not output.

[Table 3 Terminal Functions (2/4)]

PIN No.	PIN Name	In/Out (*1)	Init (*2)	Function Description	Power Supply System (*4)	I/O Type
26	YVSO/BDO1	O	Low	BT601 YcbCr data [1] / RGB V Sync output	a	D
27	YHSO/BDO0	O	Low	BT601 YcbCr data [0] / RGB H Sync output	a	D
28	GND	G	-	Ground	a,b	-
29	YCKO/RGBCKO	O	Low	BT601 Clock output / RGB Clock output	a	D
30	VDDIO	P	-	IO power source	a	-
31	GDO7	O	Low	RGB G data [7] output	a	D
32	GDO6	O	Low	RGB G data [6] output	a	D
33	GDO5	O	Low	RGB G data [5] output	a	D
34	GDO4	O	Low	RGB G data [4] output	a	D
35	VDDIO	P	-	IO power source	a	-
36	YCKI/GDO3	I/O	In	BT656 Clock input / RGB G data [3] output (*5)	a	F
37	GND	G	-	Ground	a,b	-
38	YHSI/GDO2	I/O	In	BT656 H Sync input / RGB G data [2] output (*5)	a	E
39	YVSI/GDO1	I/O	In	BT656 V Sync input / RGB G data [1] output (*5)	a	E
40	YFLDI/GDO0	I/O	In	BT601 Field input / RGB G data [0] output	a	E
41	VDD	P	-	CORE power source	-	-
42	YDI0/RDO7	I/O	In	BT656 Y data [0] input / RGB R data [7] output (*5)	a	E
43	YDI1/RDO6	I/O	In	BT656 Y data [1] input / RGB R data [6] output (*5)	a	E
44	YDI2/RDO5	I/O	In	BT656 Y data [2] input / RGB R data [5] output (*5)	a	E
45	VDDIO	P	-	IO power source	a	-
46	YDI3/RDO4	I/O	In	BT656 Y data [3] input / RGB R data [4] output (*5)	a	E
47	YDI4/RDO3	I/O	In	BT656 Y data [4] input / RGB R data [3] output (*5)	a	E
48	YDI5/RDO2	I/O	In	BT656 Y data [5] input / RGB R data [2] output (*5)	a	E
49	YDI6/RDO1	I/O	In	BT656 Y data [6] input / RGB R data [7] output (*5)	a	E
50	YDI7/RDO0	I/O	In	BT656 Y data [7] input / RGB R data [0] output (*5)	a	E

* Fix an unused input pin to GND or VDDIO (Fix SDA and SCL to I2CVDD. TEST0 and TEST1 are excluded.) .
*1) “I” shows the input, “O” shows the output, “I/O” shows the bidirection, “P” shows the power supply, and “G” shows GND.
*2) “PD” shows the pull-down, “In” shows the input mode, and “Low” shows the Low level output.
*4) "a" in the column in the power supply system shows VDDIO, "b" shows I2CVDD, "c" shows LVDD, and "d" shows PVDD.
*5) 36-50 pins direction depends on the modes.
the RGB data output mode: output
the LVDS data output mode: input

[Table 3 Terminal Functions (3/4)]

PIN No.	PIN Name	In/Out (*1)	Init (*2)	Function Description	Power Supply System (*4)	I/O Type
51	GND	G	-	Ground	a,b	-
52	I2CDEV	I	-	I^2C device address setting	a	A
53	RGBMUTE	I	-	MUTE signal : High active	a	B
54	MIR_EN	I	-	LVDS data mirror enable : High active	a	A
55	TEST0	I	PD	Test pin 0 (*3) (Connect to GND)	a	C
56	TEST1	I	PD	Test pin 1 (*3) (Connect to GND)	a	C
57	RESETB	I	-	Logic reset signal: Low active	a	B
58	LPDNB	I	-	LVDS reset signal: Low active	a	B
59	VDDIO	P	-	IO power source	a	-
60	PGND	G	-	PLL ground	d	-
61	PVDD	P	-	PLL ground	d	-
62	LGND	G	-	LVDS ground	c	-
63	TDP	O	-	LVDS data output D ch P	c	I
64	TDN	O	-	LVDS data output D ch N	c	I
65	TCKP	O	-	LVDS clock output P	c	I
66	TCKN	O	-	LVDS clock output N	c	I
67	TCP	O	-	LVDS data output C ch P	c	I
68	TCN	O	-	LVDS data output C ch N	c	I
69	LGND	G	-	LVDS ground	c	-
70	LVDD	P	-	LVDS power source	c	-
71	TBP	O	-	LVDS data output B ch P	c	I
72	TBN	O	-	LVDS data output B ch N	c	I
73	TAP	O	-	LVDS data output A ch P	c	I
74	TAN	O	-	LVDS data output A ch N	c	I
75	LGND	G	-	LVDS ground	c	-

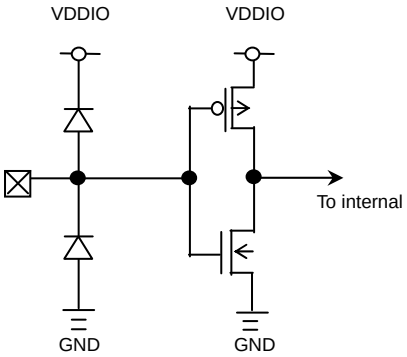
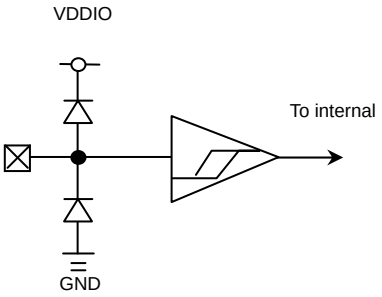
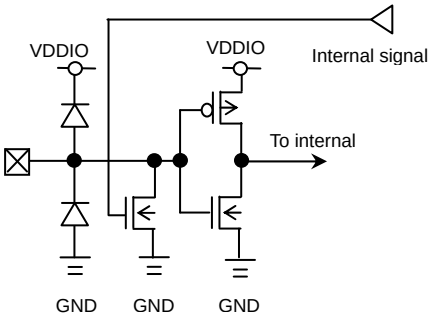
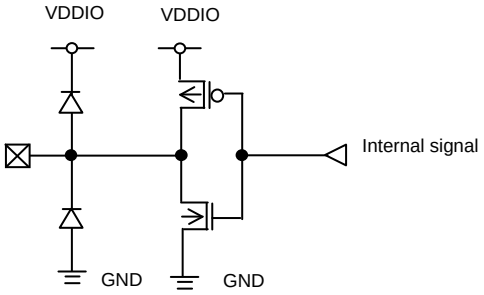
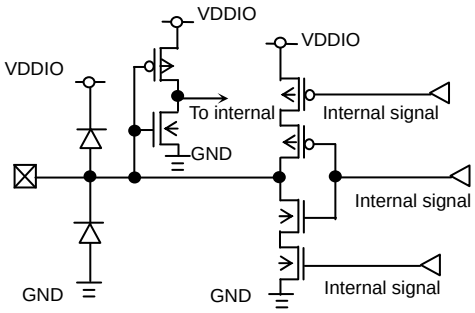
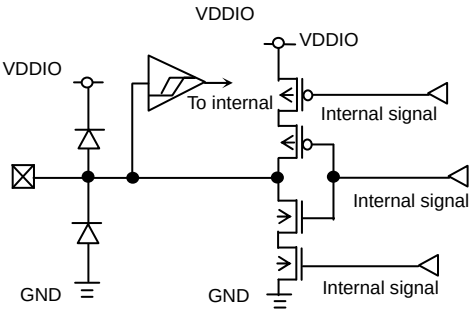
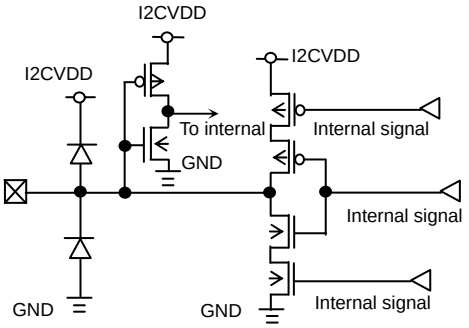
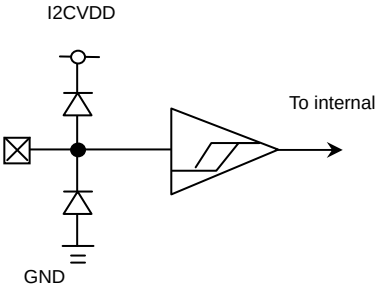
* Fix an unused input pin to GND or VDDIO (Fix SDA and SCL to I2CVDD. TEST0 and TEST1 are excluded.) .
*1) “I” shows the input, “O” shows the output, “I/O” shows the bidirection, “P” shows the power supply, and “G” shows GND.
*2) “PD” shows the pull-down, “In” shows the input mode, and “Low” shows the Low level output.
*3) Fix TEST0 and TEST1 to GND (The opening is a prohibition of use)
*4) "a" in the column in the power supply system shows VDDIO, "b" shows I2CVDD, "c" shows LVDD, and "d" shows PVDD.

[Table 3 Terminal Functions (4/4)]

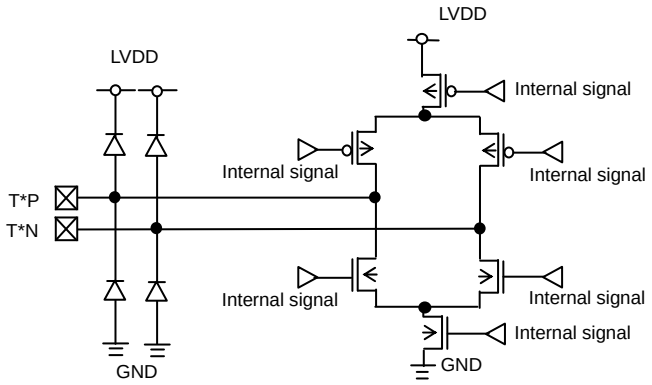
PIN No.	PIN Name	In/Out (*1)	Init (*2)	Function Description	Power Supply System (*4)	I/O Type
76	GND	G	-	Ground	a,b	-
77	RDI0	I	-	RGB R data [0] input	a	A
78	RDI1	I	-	RGB R data [1] input	a	A
79	RDI2	I	-	RGB R data [2] input	a	A
80	RDI3	I	-	RGB R data [3] input	a	A
81	RDI4	I	-	RGB R data [4] input	a	A
82	RDI5	I	-	RGB R data [5] input	a	A
83	RDI6	I	-	RGB R data [6] input	a	A
84	RDI7	I	-	RGB R data [7] input	a	A
85	VDDIO	P	-	IO power source	a	-
86	GDI0	I	-	RGB G data [0] input	a	A
87	GDI1	I	-	RGB G data [1] input	a	A
88	GND	G	-	GND	a,b	-
89	GDI2	I	-	RGB G data [2] input	a	A
90	GDI3	I	-	RGB G data [3] input	a	A
91	GDI4	I	-	RGB G data [4] input	a	A
92	GDI5	I	-	RGB G data [5] input	a	A
93	GDI6	I	-	RGB G data [6] input	a	A
94	GDI7	I	-	RGB G data [7] input	a	A
95	VDD	P	-	CORE power source	-	-
96	BDI0	I	-	RGB B data [0] input	a	A
97	BDI1	I	-	RGB B data [1] input	a	A
98	BDI2	I	-	RGB B data [2] input	a	A
99	BDI3	I	-	RGB B data [3] input	a	A
100	VDDIO	P	-	IO power source	a	-

* Fix an unused input pin to GND or VDDIO (Fix SDA and SCL to I2CVDD. TEST0 and TEST1 are excluded.) .
*1) “I” shows the input, “O” shows the output, “I/O” shows the bidirection, “P” shows the power supply, and “G” shows GND.
*2) “PD” shows the pull-down, “In” shows the input mode, and “Low” shows the Low level output.
*4) "a" in the column in the power supply system shows VDDIO, "b" shows I2CVDD, "c" shows LVDD, and "d" shows PVDD.

[Table 4 (1/2)]

Type	Equivalent circuit configuration	Type	Equivalent circuit configuration
A	 Input terminal	B	 Input terminal with schmitt
C	 Input terminal with pull down	D	 Output terminal
E	 Input/Output terminal	F	 Input/Output terminal with schmitt
G	 Input/Output terminal (2-line serial I/F)	H	 Input terminal with schmitt (2-line serial I/F)

[Table 4 (2/2)]

Type	Equivalent circuit configuration
I	 Output terminal (LVDS)

●Pin configurations

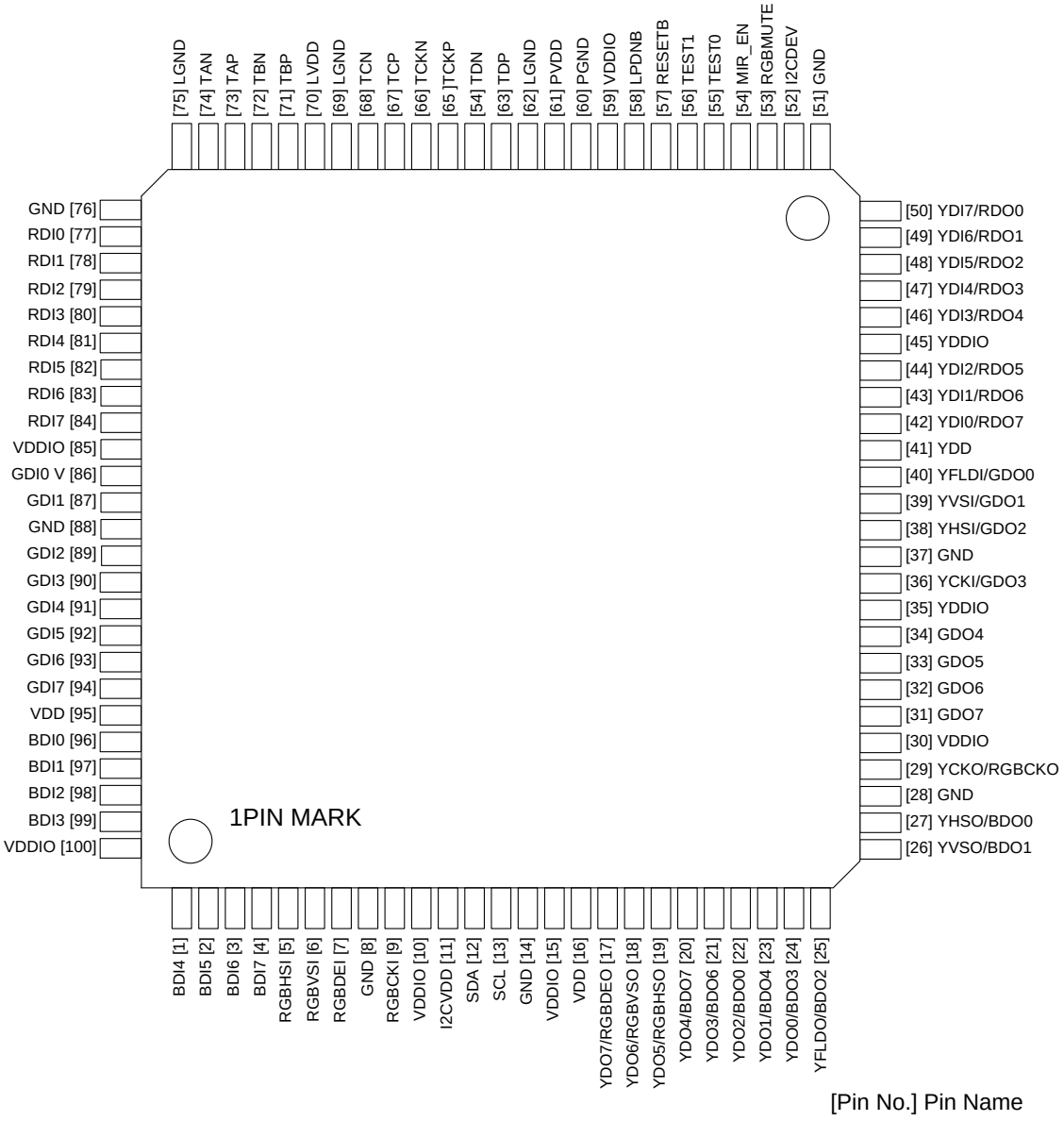


Fig.2 Pin configurations

●Electrical characteristics (DC)

[Table 5]

Unless otherwise specified, VDD=1.80V, VDDIO=3.3V, I2CVDD=3.3V, PVDD=3.3V, LVDD=3.3V, GND=0.0V, Ta=25℃, fIN=36MHz

Parameter	Symbol	Limits			Unit	Condition	
		Min.	Typ.	Max.			
Input frequency 1	FIN1	8.0	-	36.0	MHz	RGBCKI	
Input frequency 2	FIN2	8.0	-	55.0	MHz	YCKI	
Input clock duty	DCKI	45	50	55	%	RGBCKI, YCKI	
Operational current	IDD1	-	16	-	mA	36MHz (VDD)	
LVDS supply current	ILVDD1	-	55	-	mA	36MHz, LVDS_RS = 1 (LVDD, PVDD) Input toggle pattern (Fig.4)	
LVDS supply current	ILVDD2	-	38	-	mA	36MHz, LVDS_RS = 0 (LVDD, PVDD) Input toggle pattern (Fig.4)	
Leakage current	IDDst1	-	-	50	μA	Release reset , input pin =GND (VDD)	
Input ”H” current	IIH	-10	-	10	μA	VIH=IO_LVL	
Input ”L” current	IIL	-10	-	10	μA	VIL=GND	
Pull-down current	IPD	25	50	100	μA	VIH=IO_LVL	
Input ”H” voltage 1	VIH1	IO_LVL x0.8	-	IO_LVL +0.3	V	Normal input (Including input mode of I/O terminal)	
Input ”L” voltage 1	VIL1	-0.3	-	IO_LVL x 0.2	V	Normal input (Including input mode of I/O terminal)	
Input ”H” voltage 2	VIH2	IO_LVL x0.85	-	IO_LVL +0.3	V	Hysteresis input (RESETB, RGBCKI, YCKI, LPDNB, SCL, RGBMUTE)	
Input ”L” voltage 2	VIL2	-0.3	-	IO_LVL x 0.15	V	Hysteresis input (RESETB, RGBCKI, YCKI, LPDNB, SCL, RGBMUTE)	
Output ”H” voltage	VOH	IO_LVL -0.4	-	IO_LVL	V	IOH=-1.0mA(DC) (including output mode of I/O terminal)	
Output ”L” voltage	VOL	0.0	-	0.4	V	IOL=1.0mA(DC) (including output mode of I/O terminal)	
LVDS Transmitter							
Differential output voltage	VOD	250	350	450	mV	RL=100Ω	Normal Swing LVDS_RS(*1) = 1
		120	200	300	mV		Reduced Swing LVDS_RS(*1) = 0
Change in VOD between complementary output states	ΔVOD	-	-	35	mV	RL=100Ω	
Common mode voltage	VOC	1.125	1.25	1.375	V		
Change in VOC between complementary output states	ΔVOC	-	-	35	mV		
Output short circuit current	IOS	-	-	-24	mA	VOUT(*2)=0V, RL=100Ω	
Output TRI-STATE current	IOZ	-	-	±10	μA	LPDNB=GND VOUT(*2)=GND to LVDD	

* IO_LVL is a generic name of VDDIO, VDDI2C.

(*1) LVDS_RS is a register name controlled with 2-line serial interface.

(*2) VOUT=TAN/P, TBN/P, TCN/P, TDN/P, TCKN/P

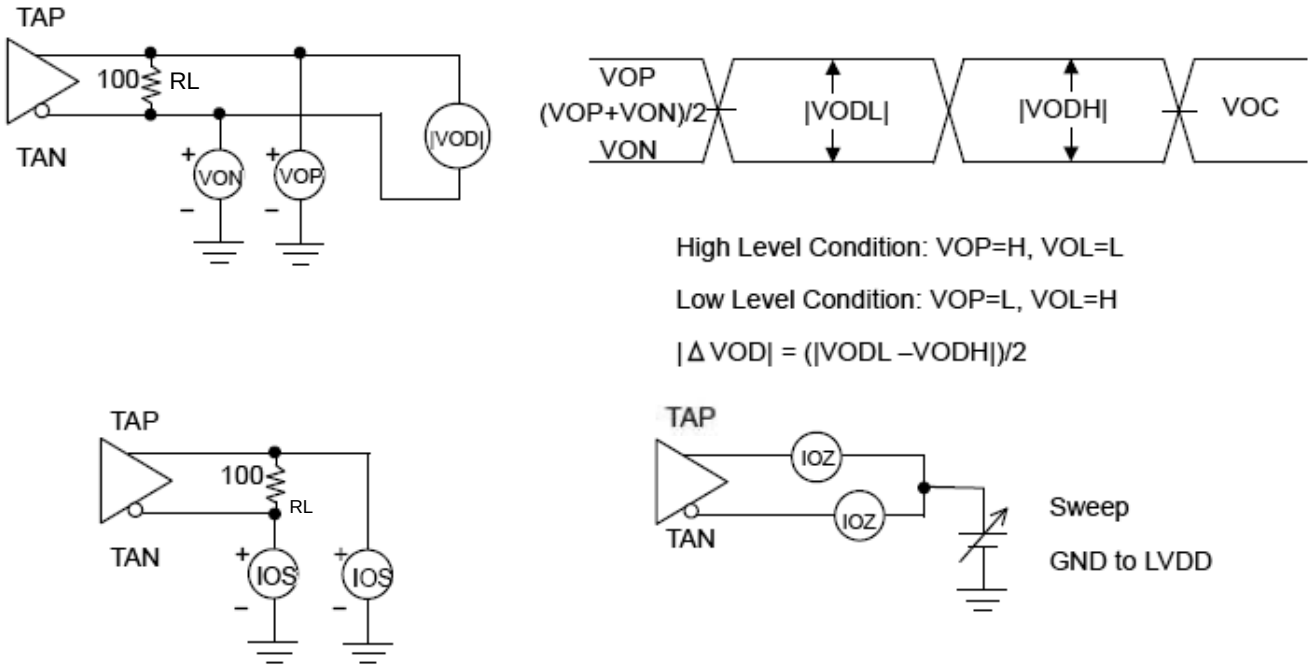
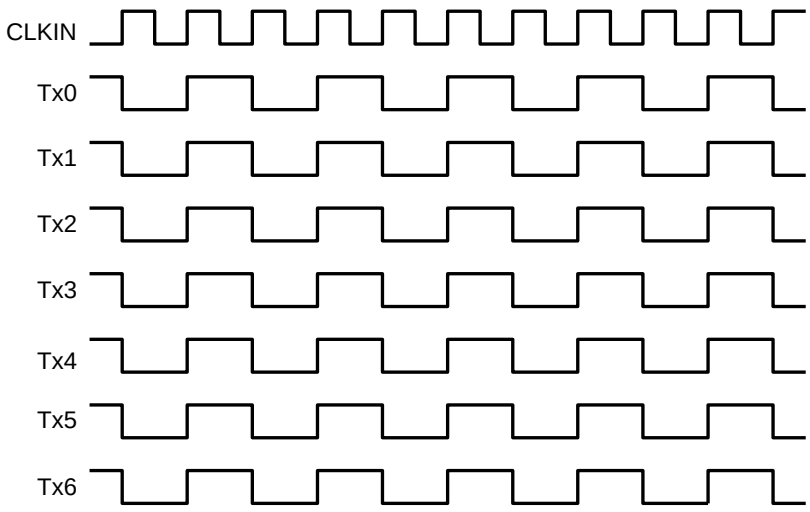


Fig.3 LVDS Transmitter characteristic diagram



X=A,B,C,D

※Input waveform to the LVDS transmitter block

※Tx0-7 are the data before being serialized by the LVDS transmitter.
Refer to Fig.8 for the serialized data sequence.

Fig.4 Input toggle pattern

●Electric Characteristics (AC)

1. Image quality adjustment data input interface timing

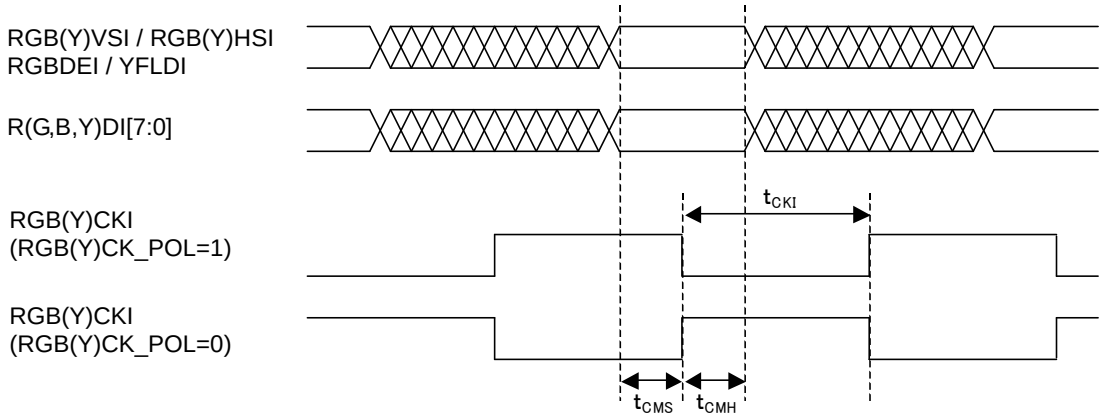


Fig.5 Data input interface timing

[Table 6]
Unless otherwise specified, VDD=1.80V, VDDIO=3.3V, I2CVDD=3.3V, PVDD=3.3V, LVDD=3.3V, GND=0.0V, Ta=25℃

Symbol	Description	Min.	Typ.	Max.	Unit
t_{CKI1}	RGBCKI Clock Cycle	27.7	-	125	ns
t_{CKI2}	YCKI Clock Cycle	18.1	-	125	ns
d_{CKI}	RGB(Y)CKI Clock Duty	45	50	55	%
t_{CMS}	RGB(Y)CKI Rise / Fall set-up Time	6	-	-	ns
t_{CMH}	RGB(Y)CKI Rise / Fall Hold Time	5	-	-	ns

* RGB(Y)CK_POL is an internal register of BU1523KV to determine the polarity of RGB(Y)CKI.
* Ensure to make the total number of 1 line input pixels to YCbCr interface to be even (multiple of 4, in case of cycles).

2. Image quality adjustment data output interface timing

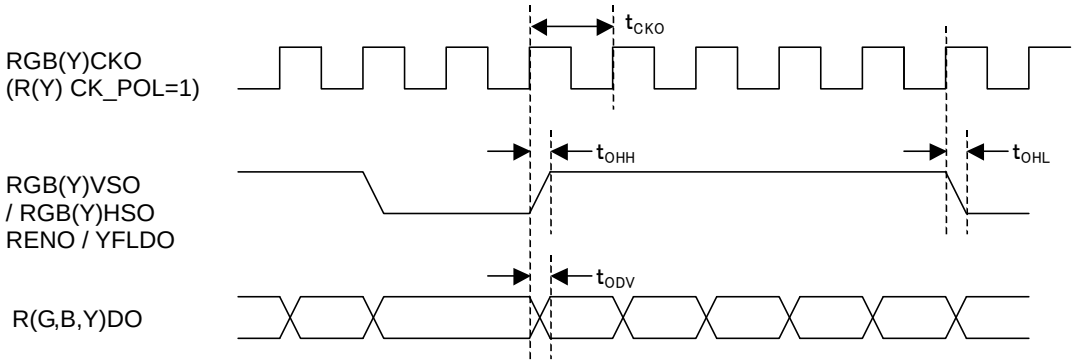


Fig.6 Data output interface timing

[Table 7]
Unless otherwise specified, VDD=1.80V, VDDIO=I2CVDD=PVDD=LVDD=3.3V, GND=0.0V, Ta=25℃

Symbol	Description	Min.	Typ.	Max.	Unit
t_{CKO1}	RGBCKO Clock Cycle	27.7	-	125	ns
t_{CKO2}	YCKO Clock Cycle	18.1	-	125	ns
d_{CKO1}	RGBCKO Clock Duty	40	50	60	%
d_{CKO2}	YCKO Clock Duty	35	50	65	%
t_{ODV}	Output delay R(G, B,Y)DO	-	-	5	ns
t_{OHL}, t_{OHH}	Output delay RGB(Y)VSO, RGB(Y)HSO, RENO/YFLDO	-	-	5	ns

* The above figure shows the waveform when RGB(Y)CK_POL= “1” is set. When RGB(Y)CK_POL= “0” is set, RGB(Y)VSO, RGB(Y)HSO and RGB(Y)DO are output at the falling edge of RGB(Y)CKO.

3. LVDS transmitter switching characteristic

[Table 8]

Unless otherwise specified, VDD=1.80V, VDDIO=I2CVDD=PVDD=LVDD=3.3V, GND=0.0V, Ta=25℃, fIN=36MHz

Symbol	Description	MIN	TYP	MAX	Unit
tLVT	LDVS Transition Time	-	0.6	1.5	ns
tTOP1	Output Data Position 0	-1.2	0.0	+1.2	ns
tTOP0	Output Data Position 1	$\frac{t_{CKI}}{7}$ -1.2	$\frac{t_{CKI}}{7}$	$\frac{t_{CKI}}{7}$ +1.2	ns
tTOP6	Output Data Position 2	$2\frac{t_{CKI}}{7}$ -1.2	$2\frac{t_{CKI}}{7}$	$2\frac{t_{CKI}}{7}$ +1.2	ns
tTOP5	Output Data Position 3	$3\frac{t_{CKI}}{7}$ -1.2	$3\frac{t_{CKI}}{7}$	$3\frac{t_{CKI}}{7}$ +1.2	ns
tTOP4	Output Data Position 4	$4\frac{t_{CKI}}{7}$ -1.2	$4\frac{t_{CKI}}{7}$	$4\frac{t_{CKI}}{7}$ +1.2	ns
tTOP3	Output Data Position 5	$5\frac{t_{CKI}}{7}$ -1.2	$5\frac{t_{CKI}}{7}$	$5\frac{t_{CKI}}{7}$ +1.2	ns
tTOP2	Output Data Position 6	$6\frac{t_{CKI}}{7}$ -1.2	$6\frac{t_{CKI}}{7}$	$6\frac{t_{CKI}}{7}$ +1.2	ns
tPLL	Phase Locked Loop Set Time	-	-	10.0	ms

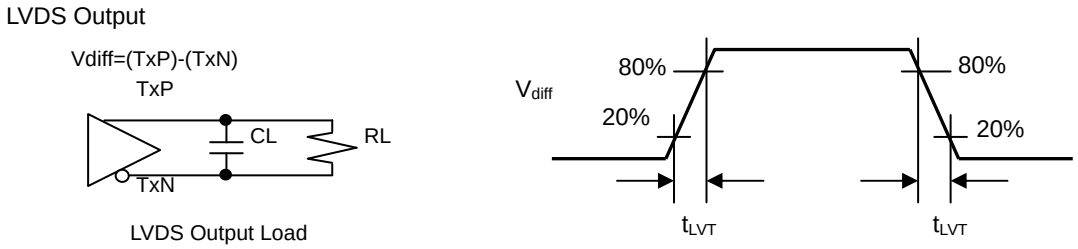


Fig.7 LVDS Output AC Timing diagram 1

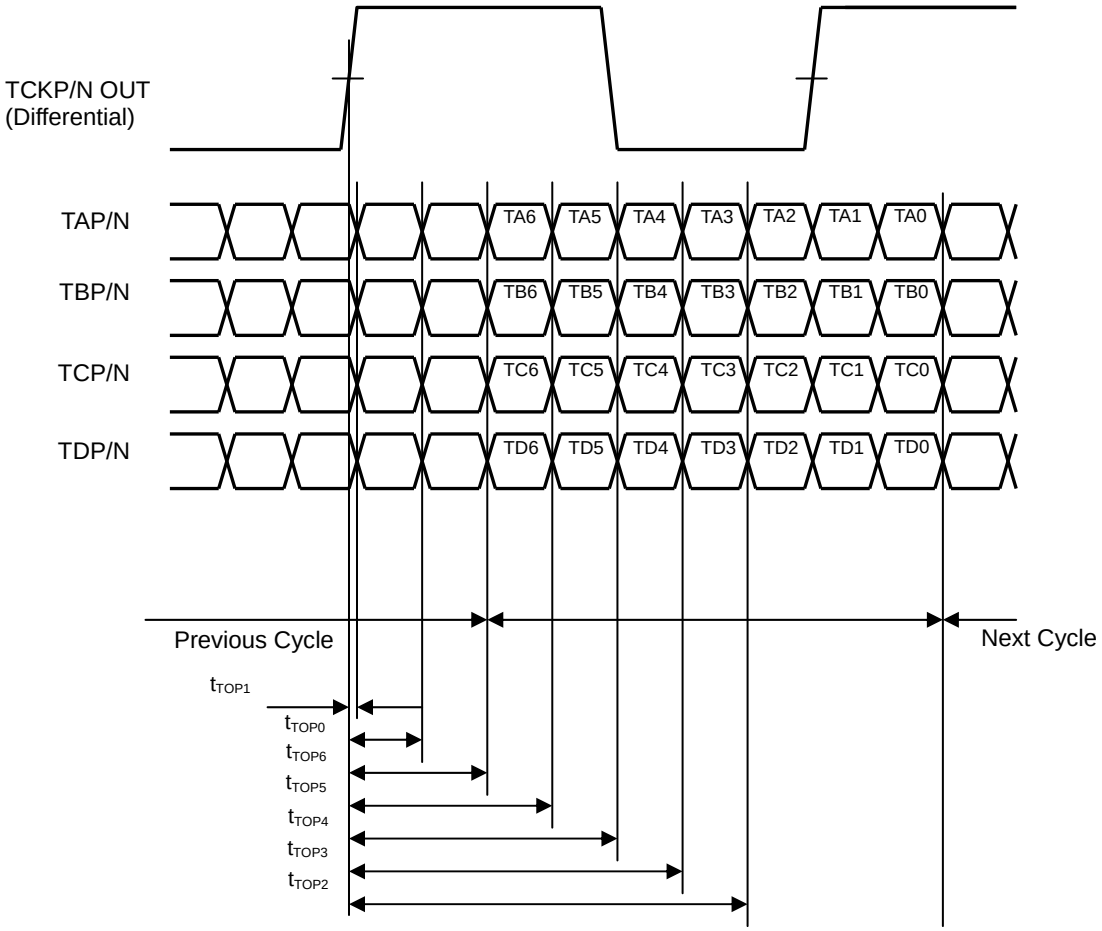
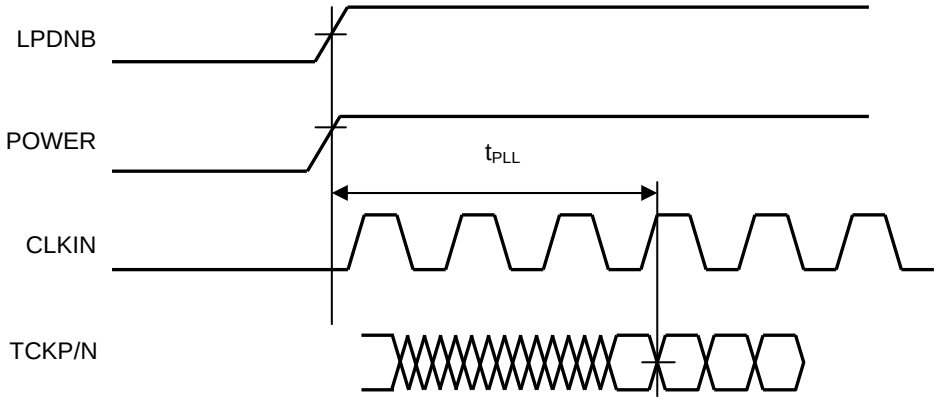


Fig.8 LVDS Output AC Timing diagram 2



* POWER shows VDDIO, I2CVDD, VDD, LVDD, PVDD
* CLKIN is a clock input to the LVDS transmitter.

Fig.9 LVDS Phase Locked Loop Set Time

4. 2-line serial interface timing

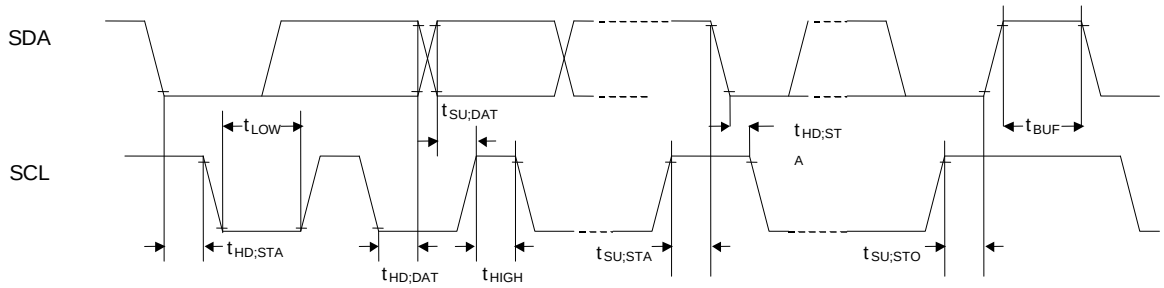


Fig.10 2-line serial interface timing

[Table 9]
Unless otherwise specified, VDD=1.80V, VDDIO=3.3V, I2CVDD=3.3V, PVDD=3.3V, LVDD=3.3V, GND=0.0V, Ta=25℃

Symbol	Description	MIN	TYP	MAX	Unit
f_{SCL}	SDL clock frequency	0	-	400	kHz
$t_{HD;STA}$	Holding time(Repetition) ”START” Condition After this period, the first clock pulse is generated.	0.6	-	-	µs
t_{LOW}	Low period of SDL clock	1.3	-	-	µs
t_{HIGH}	High period of SDL clock	0.6	-	-	µs
$t_{SU;STA}$	Setup time of repetition ”START” condition	0.6	-	-	µs
$t_{HD;DAT}$	Data hold time	0			µs
$t_{SU;DAT}$	Data setup time	100	-	-	ns
$t_{SU;STO}$	Setup time of 'STOP' condition	0.6	-	-	µs
t_{BUF}	'Bus free time between STOP' condition and 'START' condition	1.3	-	-	µs

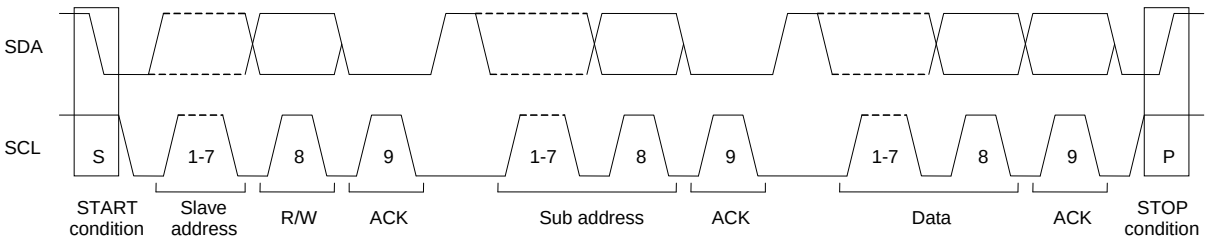
●Operation explanation of each block

1. Image quality adjustment of RGB interface
   It adjusts image quality input through 24-bit RGB interface.
   The supported I/O interface consists of 24-bit data, vertical synchronization signal, horizontal synchronization signal and data enable signal. It converts 24-bit RGB into YCbCr444 and makes adjustment on the contrast, brightness, sharpness, hue and intensity in the YCbCr space. The contrast, brightness and sharpness are adjusted against the luminance (Y) component and the hue and intensity are adjusted against the color difference (CbCr) component. In addition to the image quality adjustment in the YCbCr space, it is also equipped with the RGB independent gamma correction capability in the RGB space. Converting YCbCr444 to 24-bit RGB, gamma correction is made to each of the RGB components. 16 gamma curve points can be set and the intervals between those set points are linearly interpolated. When the RGBMUTE terminal is set to “High” level, the RGB output data will be all “0” from the next frame.

2. Image quality adjustment of YUV
   It adjusts image quality input through YCbCr422 interface.
   The supported I/O interfaces are ITU-R BT.656-4 and YCbCr with synchronization signal (complied with ITU-R BT.601). When the input is ITU-R BT.656-4, the output can be selected from ITU-R BT.656-4 and YCbCr with synchronization signal. However, when the input is YCbCr with synchronization signal, the output can only be YCbCr with synchronization signal. It makes adjustment on the contrast, brightness, sharpness, hue and intensity in the YCbCr space. The contrast, brightness and sharpness are adjusted against the luminance (Y) component and the hue and intensity are adjusted against the color difference (CbCr) component.

3. LVDS transmitter
   It outputs high-speed serial data for image quality adjustment of RGB interface in LVDS format. The data mapping to be output in the LVDS format can be changed by the register setting. When the LPDNB terminal is set to “Low” level, the LVDS transmitter part will go into power down mode. The LVDS output will become Hi-Z status.

4. 2-line serial interface
   2-line serial interface slave function is embedded. The registers are accessed through this interface. The slave address is 46h (in 7-bit notation) when I2CDEV=0 and 47h (in 7-bit notation) when I2CDEV=1. The sub address is automatically incremented when consecutively accessed twice or more in read or write operation. * Slave address of 46h and 47h are in hexadecimal. * Fig.11 depicts the status when I2CDEV=0.



Data sending and receiving waveform

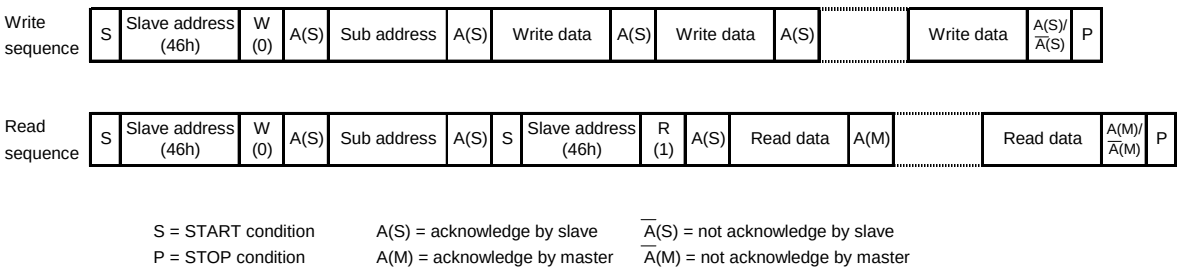
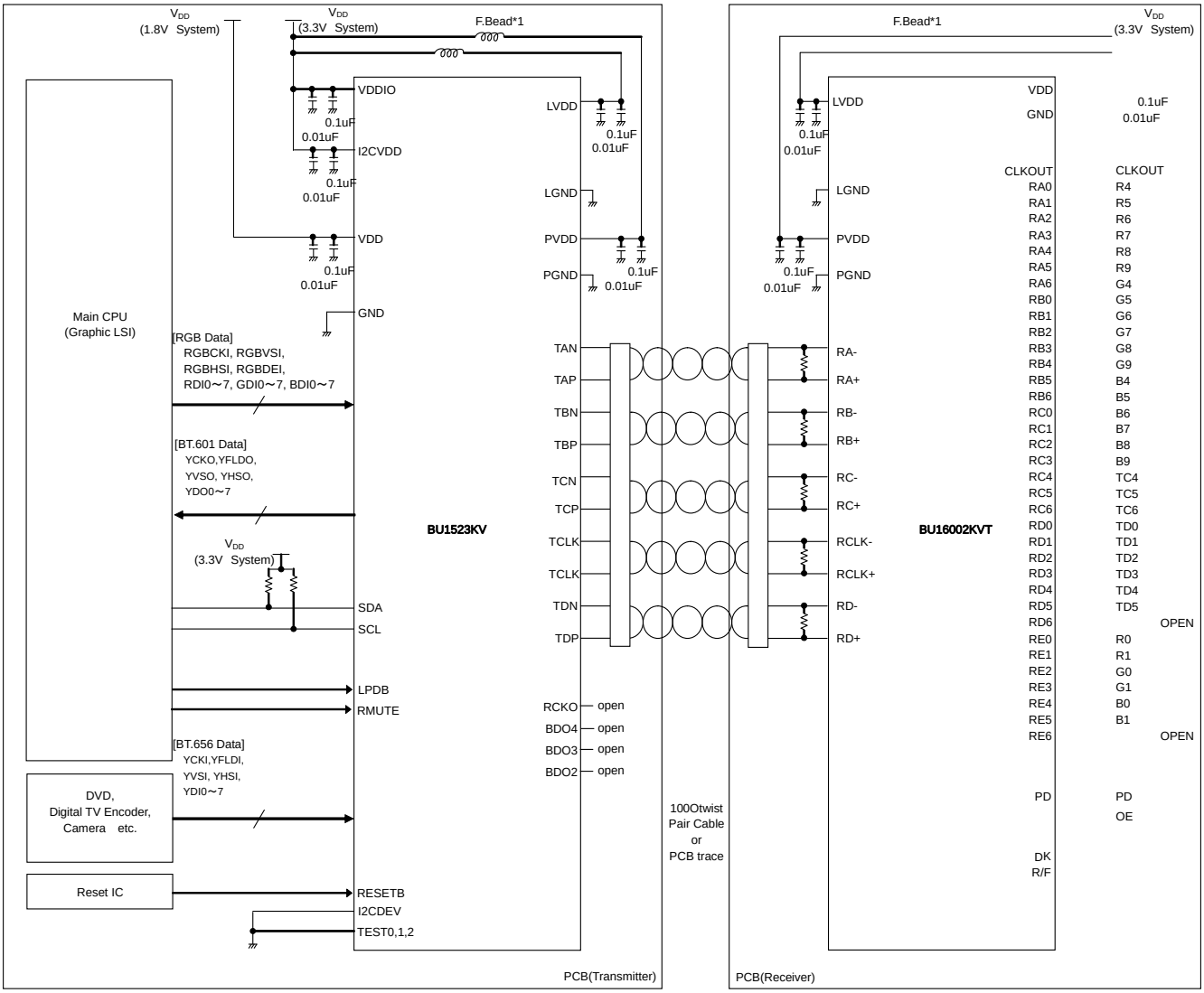


Fig.11 2-line serial interface format

●Example of application circuit



*1: Recommended Parts: F.Bead: BLM18A-Series (Murata Manufacturing)
*2: If LVDS_RS is tied to “1”, LVDS swing is 350m V. If LVDS_RS is tied to “0”, LVDS swing is 200m V.

Fig.12 BU1523KV System connection Diagram

The above figure is an example of system connection for reference only and not intended to guarantee operation.

●Procedure for turning on power supply

Follow the power-on sequence of VDD→(VDDIO, I2CVDD, PVDD, LVDD) as depicted in Fig.13. The timing for power-on sequence is shown in Table 10 however, it is recommended to make the intervals of t_{PWUV2}, t_{PWUV} and t_{PWUVL} as short as possible. Until after voltage is applied to all the power sources, the levels of all the input pins are fixed and the low level is input onto RESETB, the internal status and pins remain unstable. Remove the reset after inputting the clock (RGBCKI, YCKI). When the clock (RGBCKI, YCKI) is to be temporarily halted during the operation, apply the reset after the clock (RGBCKI, YCKI) stopped to fix the operation, then follow the power-on sequence and remove the reset after inputting the clock (RGBCKI, YCKI). 2-line serial interface is enabled for communication after the reset (RESETB) is removed. However, racing may be caused if the rising edge of the reset (RESETB) signal and the signal change of 2-line serial interface occur at the same time. Ensure not to allow the rising edge of the reset (RESETB) signal and the signal change of 2-line serial interface to occur at the same time. Design the system to avoid racing and system malfunction when the internal status and pins are unstable.

* The reset is also possible by the software reset (SRST_R_IP, SRST_Y_IP, SRST_LVDS).

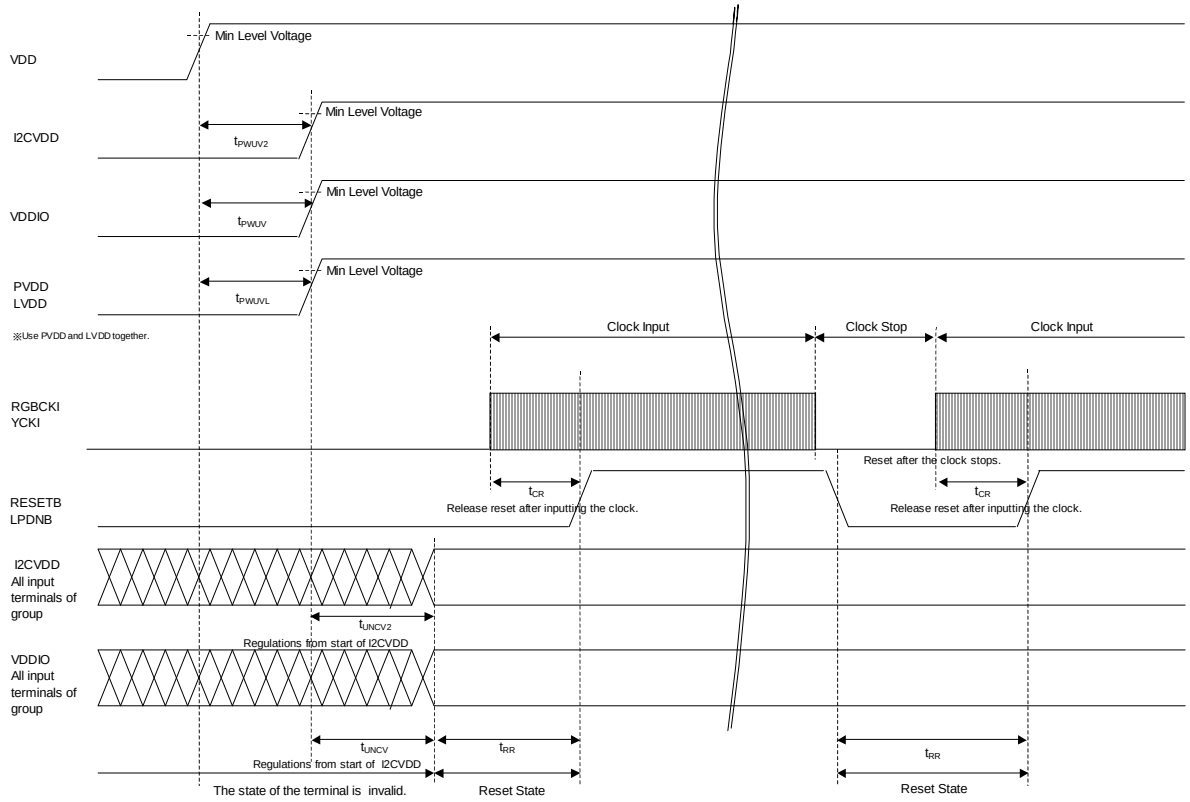


Fig.13 Power supply input procedure (Min level is power-supply voltage lower bound of recommended range.)

[Table 10 Recommended value at time to turn on power supply]

Item	Min.	Max.	Unit
t_{PWUV2}	0	50	ms
t_{PWUV}	0	50	ms
t_{PWUVL}	0	50	ms
t_{UNCV2}	0	1	ms
t_{UNCV}	0	1	ms
t_{RR}	1	-	ms
t_{CR}	0.1	-	ms

The power-off sequence is reverse of the power-on sequence, in the order of (VDDIO, I2CVDD, PVDD, LVDD)→VDD as depicted in Fig.14. The timing for power-off sequence is shown in Table 11, however, it is recommended to make the intervals of t_{PWDV2m}, t_{PWDV} and t_{PWDVL} as short as possible.
Note that turning off from the VDD (Power to the internal CORE) makes the internal status and pin status unstable.

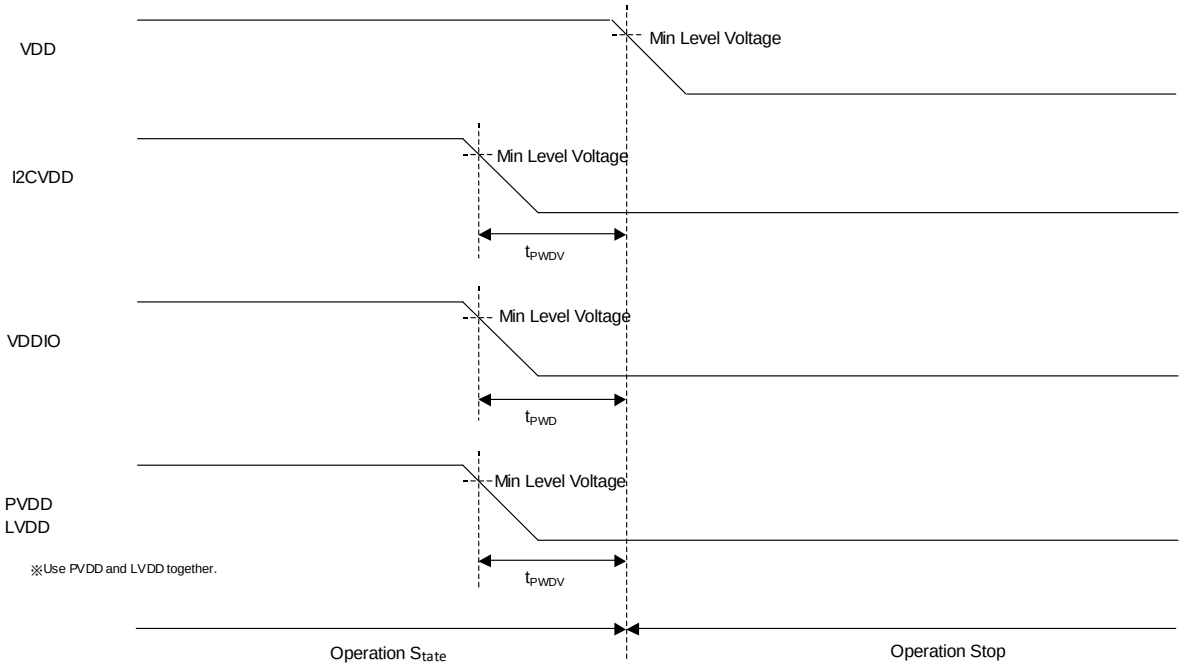


Fig.14 Power-off procedure (Min level is power-supply voltage lower bound of recommended range of motion.)

[Table 11 Power-off time recommended value]

Item	Min.	Max.	Unit
t_{PWDV2}	0	50	ms
t_{PWDV}	0	50	ms
t_{PWDVL}	0	50	ms

●PCB Design Guideline for LVDS

- Interconnecting media between Transmitter and Receiver (i.e.PCB trace, connector, and cable) should be well balanced. (Keep all these differential impedance and the length of media as same as possible.).
- Locate by –pass capacitors adjacent to the device pins as close as possible.
- Minimize the distance between traces of a pair. (S1) to maximize common mode rejection. See following figure.
- Place adjacent LVDS trace pair at least twice (>2 x S1) as far away.
- Avoid 90 degree bends.
- Minimize the number of VIA on LVDS traces.
- Match impedance of PCB trace, connector, media (cable) and termination to minimize reflections (emissions) for cabled applications (typically 100Ω Differential mode characteristic impedance).

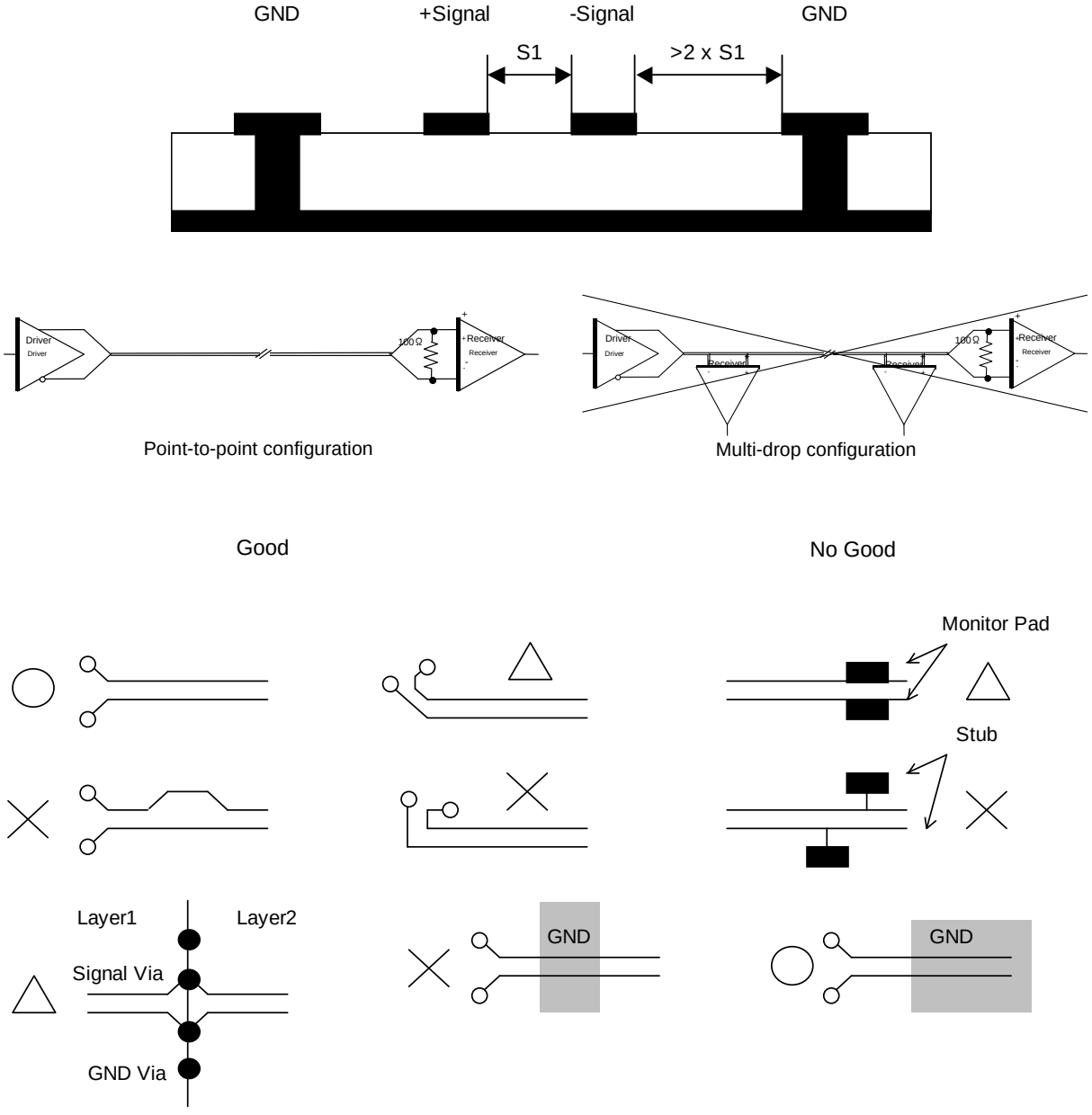


Fig.15 PCB Design Guideline for LVDS

●Notes for use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Recommended Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

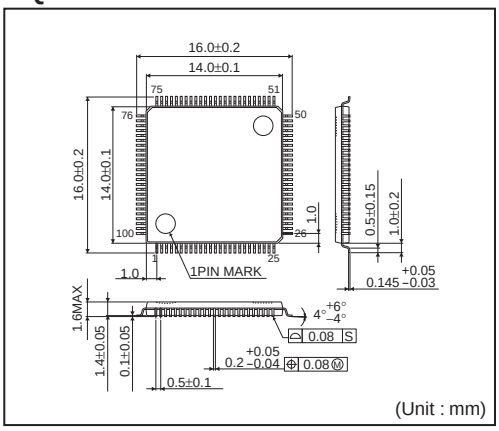
(12) Rush current
For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of wiring.

●Ordering part number

B	U	1	5	2	3	K	V	-	E	2

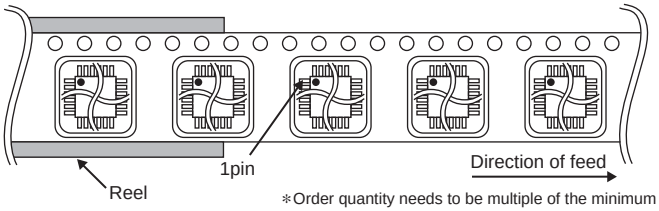
Part No. Part No. Package KV:VQFP100 Packaging and forming specification E2: Embossed tape and reel

VQFP100



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

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5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

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2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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