Title	***Engineering Prototype Report for EP-86 – 6.6 W Multi-Class Powered Device (PD) for Power over Ethernet (PoE) Using DPA-Switch® (DPA423G)***
Specification	Input: 33-57 VDC, Output: 3.3 V / 2.0 A
Application	PoE Class 2 PD – Including IEEE802.3af Compliant Interface Circuit
Author	Power Integrations Applications Department
Document Number	EPR-86
Date	April 13, 2006
Revision	1.1

Summary and Features

- Meets **IEEE802.3af** requirements according to University of New Hampshire Interoperability Consortium **(UNH-IOC**) test results, for Class 1–3 PoE PDs
- *DPA-Switch* PWM controller with integrated 220 V power MOSFET switch
  - Under-voltage (UV) and overvoltage (OV) shutdown functions
  - Auto-recovering, hysteretic thermal shutdown
  - Auto-restart function: protects against short-circuit and open loop faults
  - No-load regulation achieved by cycle skipping
  - Fully integrated soft-start minimizes start-up stress and overshoot
  - Externally programmed I_{LIMIT} scales with V_{IN} for power limiting
  - Lossless MOSFET current sense eliminates external sensing components
- Small footprint 3.1" × 1", low overall height 0.45" (excluding RJ-45 connector)

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5245 Hellyer Avenue, San Jose, CA 95138 USA.
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Important Note:
Although this board was designed to satisfy safety isolation requirements, it has not been agency approved. Therefore, please take the appropriate safety precautions.

1 Introduction

This engineering report describes a PoE power supply designed around the DPA423G. The supply can deliver 6.6 W continuously, from an input voltage range of 33 VDC to 57 VDC.

The following design information is provided: the power supply specification, circuit diagrams, a complete bill of materials, the results of the *PIXIs* spreadsheet file that was used to design the supply and detailed information on the design and construction of the transformer. Data and test results that document the performance of the supply under various line and load conditions are also included.

Figure 1 – Populated Circuit Board Top View.

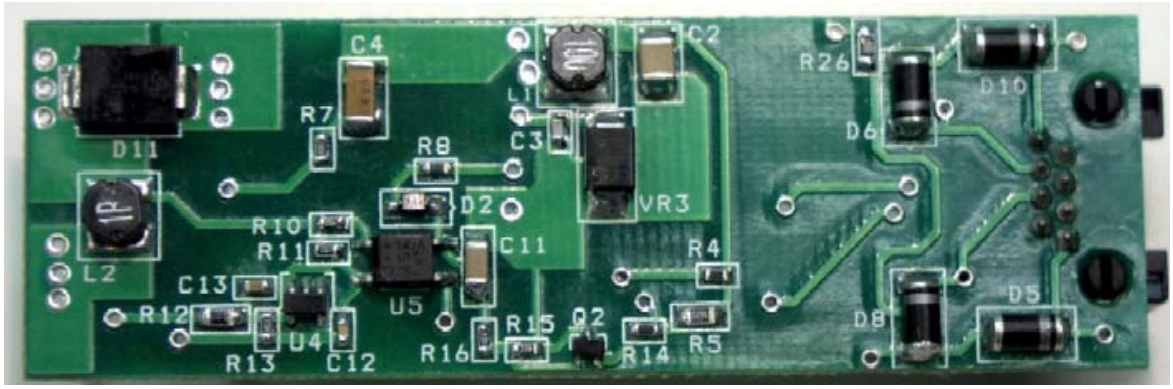

Figure 2 – Populated Circuit Board Bottom View.

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2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	33	48	57	VDC	
Under-Voltage ON	$V_{IN\_UV\_ON}$			42	VDC	
Under-Voltage OFF	$V_{IN\_UV\_OFF}$	33			VDC	
Output						
Output Voltage 1	V_{OUT1}	3.135	3.3	3.465	V	± 5%
Output Ripple Voltage 1	$V_{RIPPLE1}$			35	mVp-p	20 MHz bandwidth
Output Current 1	I_{OUT1}	0		2	A	
Output Peak Current 1	I_{OUT1_PK}	2.5			A	
Total Output Power						
Average Output Power	P_{OUT1}		6.6		W	
Average Output Power	P_{OUT_FAULT}	8.6			W	R6 = 10.2 Ω
Full Load Efficiency	η		73		%	
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Ambient Temperature	T_{AMB}	0		40	°C	

3 Schematic

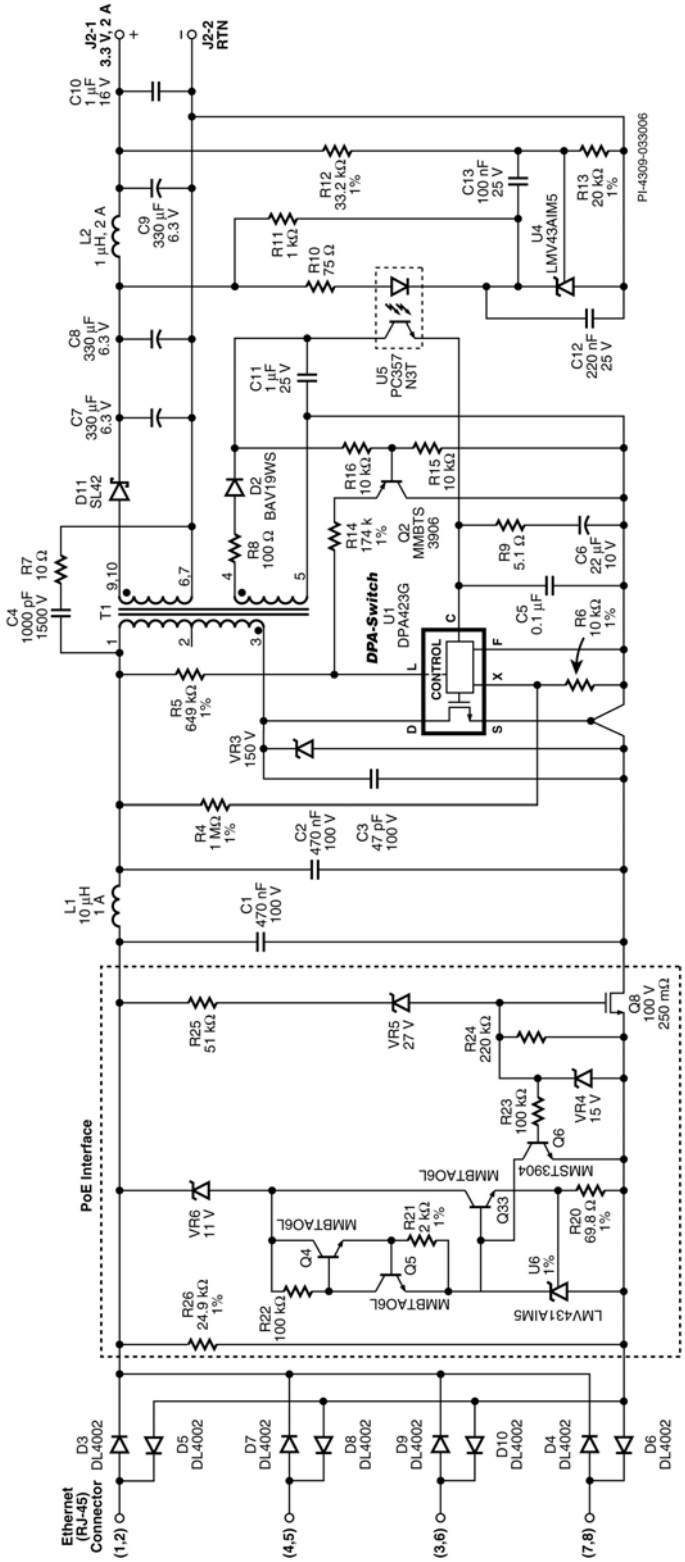

Figure 3 – Schematic.

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4 Circuit Operation

4.1 General

A flyback topology was used to minimize circuit board size, parts count and cost. This topology also provides excellent operating efficiency across the input voltage range.

4.2 DPA-Switch Primary

The DPA423G IC implements PWM control of the internal power MOSFET and initiates a soft start-up function when it first powers up. The IC also monitors die temperature as part of its over-temperature protection function and also monitors the input voltage as part of its under-voltage detection and overvoltage shutdown functions. The integrated 220 V MOSFET provides excellent switching characteristics at the selected 400 kHz operating frequency. The MOSFET and controller consume very little power, giving good efficiency across the entire input voltage operating range.

Diodes D3 through D9 ensure that the incoming DC input voltage is correctly polarized. Capacitors C1 and C2 and inductor L1 form a low-cost pi (π) filter that attenuates conducted EMI noise, to keep it from being passed to the incoming line.

Resistors R4 and R6 program the internal current limit of the DPA423G, so that it reduces as the input voltage increases. This helps to keep the variance of the maximum output overload current below 5%, across the entire input voltage range.

The IC's integrated MOSFET is protected from overvoltage stresses that could damage it (during a line surge) by a primary-side Zener diode clamp (VR3). Zener diode VR3 does not conduct under normal operating conditions.

The primary bias winding provides CONTROL pin current after start-up. Diode D2 rectifies the bias winding voltage, while R8 and C11 attenuate high frequency switching noise and reduce the peak charging of the bias voltage.

4.3 Output Rectification

The secondary winding voltage is rectified by a low-loss Schottky diode (D11). Low ESR, tantalum output capacitors, C7 and C8, filter the output voltage. The LC output filter (L2, C9 and C10) further attenuates switching noise and ripple from the output voltage.

4.4 Output Feedback

Resistor divider (R12 and R13) senses the output voltage and feeds it into the reference pin of a 1.24 V reference IC (U4). The conduction of U4 pulls current through the LED of optocoupler U5, which controls the conduction of its phototransistor (U5-B). The phototransistor modulates the current that flows into the CONTROL pin of U1. Since the *DPA-Switch* is a current-to-duty-cycle converter, it uses the varying CONTROL pin current to pulse-width modulate the duty cycle of the MOSFET switch. Resistor R10 sets the gain of U4, while R11 and C13 compensate for the variation in gain of U4 over the frequency range of the feedback loop's bandwidth (about 10 kHz). Feedback

compensation is required to ensure stable operation of the supply and optimum response to line and load transients. Capacitor C12 performs a soft-finish function that prevents the output voltage from overshooting the regulation set point during initial startup of the converter.

4.5 PoE Interface Circuit Description

See DI-88 for a full description. Resistor R26 provides the correct impedance for the detection phase of PD operation.

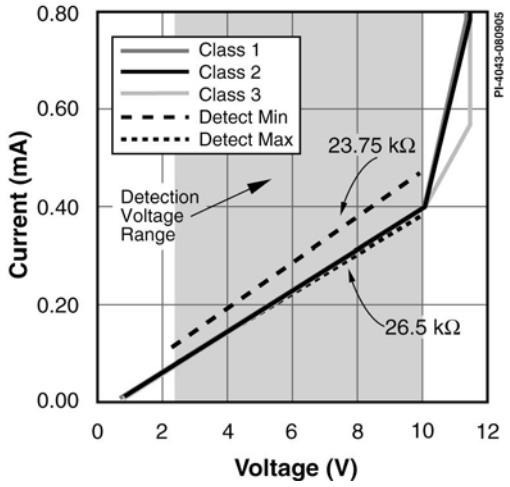

Figure 4 – Detection Impedance V-I curve.

The classification circuit is enabled when Zener diode VR6 conducts (above 11 VDC). Transistor Q9 controls the bias current source programmed to approximately 350 µA by resistor R21. This bias current source provides the minimum operating current to voltage reference IC U6. The main classification current flowing through R20 generates a voltage that is referenced to the internal reference (1.24 VDC) of U6 and that later closes the loop by controlling the base drive of Q7. The value of the classification current source is determined by the value of the voltage on the reference pin of U6 divided by the value of R20 in ohms.

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Class	P_{OUT} (min)	P_{OUT} (max)	I_{CL} (min)	I_{CL} (max)	R34
	W	W	mA	mA	Ohms
0	0.44	12.95	0.5	4	-
1	0.44	3.84	9	12	133
2	3.84	6.49	17	20	69.8
3	6.49	12.95	26	30	45.3

Figure 5 – Table of PoE Classifications and Power Levels.

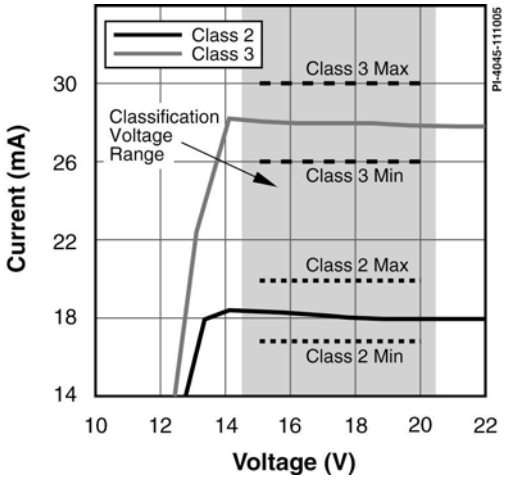

Figure 6 – Classification Current (Class 2: R34 = 69.8 Ω; Class 3: R34 = 45.3 Ω).

Zener diode VR5 conducts above 27 VDC, raising the gate voltage on the pass-switch MOSFET (Q8), turning it on when the gate-threshold voltage is exceeded. Pull-down resistor R25 limits the current through VR5 while pull-down resistor R24 keeps Q8 turned off, unless it is being actively driven on. Zener diode VR4 limits the maximum gate-to-source voltage on Q8 to 15 V. When VR5 conducts, it also turns on Q6 through R23. Transistor Q6 pulls down on the base of Q7, which turns off the main classification current source (although the bias current source of 350 µA will continue to conduct).

4.6 Wide Hysteresis Under-Voltage Lockout

If there were no other components connected to the L pin, then resistor R5 would set the under-voltage turn-on threshold to approximately 35 VDC and the turn-off threshold to approximately 33 VDC.

However, in the case of PoE, the turn-on voltage is much higher than the turn-off voltage. This requires more under-voltage hysteresis. When the power supply is operating normally, the bias voltage is approximately 14 VDC. Resistors R15 and R16 form a voltage divider that turns off the base of Q2, once the DC-DC converter has begun switching and the bias voltage is present. At start-up, when the bias voltage is absent,

Q2 is on, and sinks additional current from the resistor (R5) that connects the L pin to the DC input voltage. The value of R14 was selected so that an extra 10 µA is drawn at startup, which increases the turn-on threshold voltage to 41 VDC typical. However, because Q2 turns off after start-up, the UV turn-off threshold stays at 34 VDC (see DI-101 for more details).

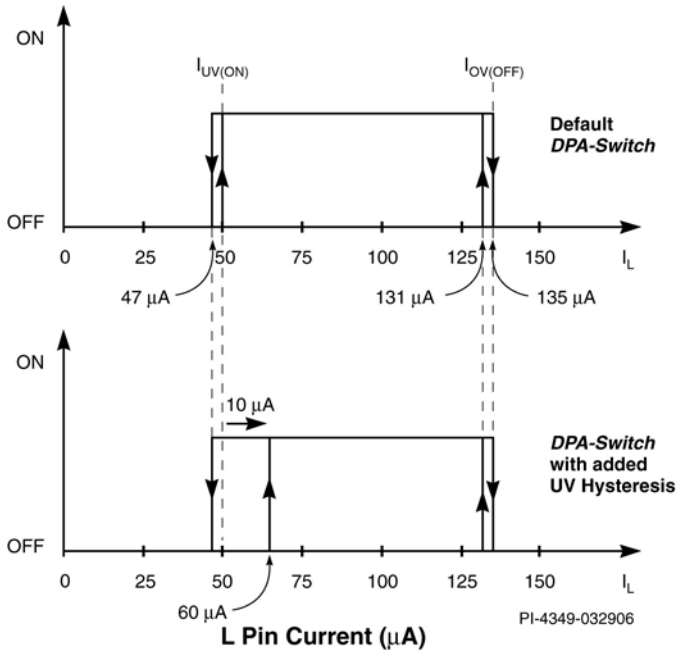

Figure 7 – L-pin current without and with the widened UV hysteresis circuit.

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5 Bill of Materials

Item	Qty.	Ref.	Description	Mfg Part Number	Mfg
1	2	C1, C2	470 nF, 100 V, Ceramic, X7R, 1210	ECJ-4YB2A474K	Panasonic
2	1	C3	47 pF, 100 V, Ceramic, NPO, 0603	06031A470JAT2A	AVX
3	1	C4	1000 pF, 1500V, 1808	1808SC102KAT1A	AVX
4	2	C5, C13	100 nF 25 V, Ceramic, X7R, 0603	ECJ-1VB1E104K	Panasonic
5	1	C6	22 µF, 10 V, Tant Electrolytic, SMD	TAJA226K010R	Kemet
6	3	C7, C8, C9	330 µF, 6.3 V, Tant Electrolytic, SMD	T495X337K006AS	Kemet
7	1	C10	1 µF, 16 V, Ceramic, X5R, 0603	GRM188R61C105KA93D	Murata
8	1	C11	1 µF, 25 V, Ceramic, X7R, 1206	ECJ-3YB1E105K	Panasonic
9	1	C12	220 nF, 25 V, Ceramic, X7R, 0603	06033D224KAT2A	AVX
10	1	D2	75 V, 0.2 A, Fast Switching, 50 ns, SOD-323	1N4148WS-7	Diode Inc.
11	8	D3, D4, D5, D6, D7, D8, D9, D10	100 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4002	Diodes Inc
12	1	D11	20 V, 4 A, Schottky, SMD, DO-214AB	SL42-9B	Vishay
13	1	J1	R/A, RJ45 Non-shielded, PCBM	RJHS-5080	Amphenol Canada
14	2	J2-1, J2-2	Zierick output pins		Zierick
15	1	L1	10 µH, 0.85 A	HM79-10100LFTR7	B.I.Technologies
16	1	L2	1 µH, 1.9 A	HM79-101R0LFTR7	B.I.Technologies
17	1	Q2	PNP, Small Signal BJT, 40 V, 0.2 A, SOT-323	MMST3906-7	Diodes Inc
18	3	Q4, Q5, Q7	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1	On Semiconductor
19	1	Q6	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-323	MMST3904	Diodes Inc
20	1	Q8	100 V, 1.15 A, 250 mΩ, N-Channel, SOT-23	SI2328DS	Vishay
21	1	R4	1.00 MΩ, 1%, 1/16 W, Metal Film, 0603	ERJ-3EKF1004V	Panasonic
22	1	R5	649 kΩ, 1%, 1/8 W, Metal Film, 0805	ERJ-6ENF6493V	Panasonic
23	1	R6	10.00 kΩ, 1%, 1/16 W, Metal Film, 0603	ERJ-3EKF1002V	Panasonic
24	1	R7	10 Ω, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ100V	Panasonic
25	1	R8	100 Ω, 1%, 1/16 W, Metal Film, 0603	ERJ-3EKF1000V	Panasonic
26	1	R9	5.1 Ω, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ5R1V	Panasonic
27	1	R10	75 Ω, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ750V	Panasonic
28	1	R11	1 kΩ, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ102V	Panasonic
29	1	R12	33.2 kΩ, 1%, 1/8 W, Metal Film, 0805	ERJ-6ENF3322V	Panasonic

30	1	R13	20 kΩ, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ203V	Panasonic
31	1	R14	174 kΩ, 1%, 1/16 W, Metal Film, 0603	ERJ-3EKF1743V	Panasonic
32	1	R15, R16	10 kΩ, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ103V	Panasonic
35	1	R20	69.8 Ω, 1%, 1/16 W, Metal Film, 0603	ERJ-3EKF69R8V	Panasonic
36	1	R21	2 kΩ, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ202V	Panasonic
37	2	R22, R23	100 kΩ, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ104V	Panasonic
38	1	R24	220 kΩ, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ224V	Panasonic
39	1	R25	51 kΩ, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ513V	Panasonic
40	1	R26	24.9 kΩ, 1%, 1/8 W, Metal Film, 0805	ERJ-6ENF2492V	Panasonic
41	1	T1	Bobbin, ER14.5/6, Horizontal, 10 pins, SMD	HM00-A5861LF DA2062-ALD SIL6029 LSTA30825 SNX1393 YC-1404S	B.I Technologies Coilcraft Hical LiShin Santronics Ying Chin
42	1	U1	*DPA-Switch*, DPA423G, SMD-8	DPA423G	Power Integrations
43	1	U4	1.24 V Shunt Regulator IC, 1%, -40 to 85 °C, SOT23-5	LMV431AIM5	National Semiconductor
44	1	U5	Optocoupler, 80 V, CTR 200-400%, 4-Mini Flat	PC357N3T	Sharp
45	1	U6	1.24 V Shunt Regulator IC, 1%, -40 to 85 °C, SOT23-5	LMV431AIM5	National Semiconductor
46	1	VR3	150 V, 5 W, 5%, DO214AC (SMB)	SMBJ150A	Diodes, Inc
47	1	VR4	15.0 V, 5%, 150 mW, SOD-323	BZT52C15T-7	Diodes, Inc
48	1	VR5	27.0 V, 5%, 150 mW, SOD-323	MAZS2700ML	Panasonic-SSG
49	1	VR6	11 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5241B-7	Diodes Inc
50	1	-	PCB, EP-86, REV B		

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6 Layout

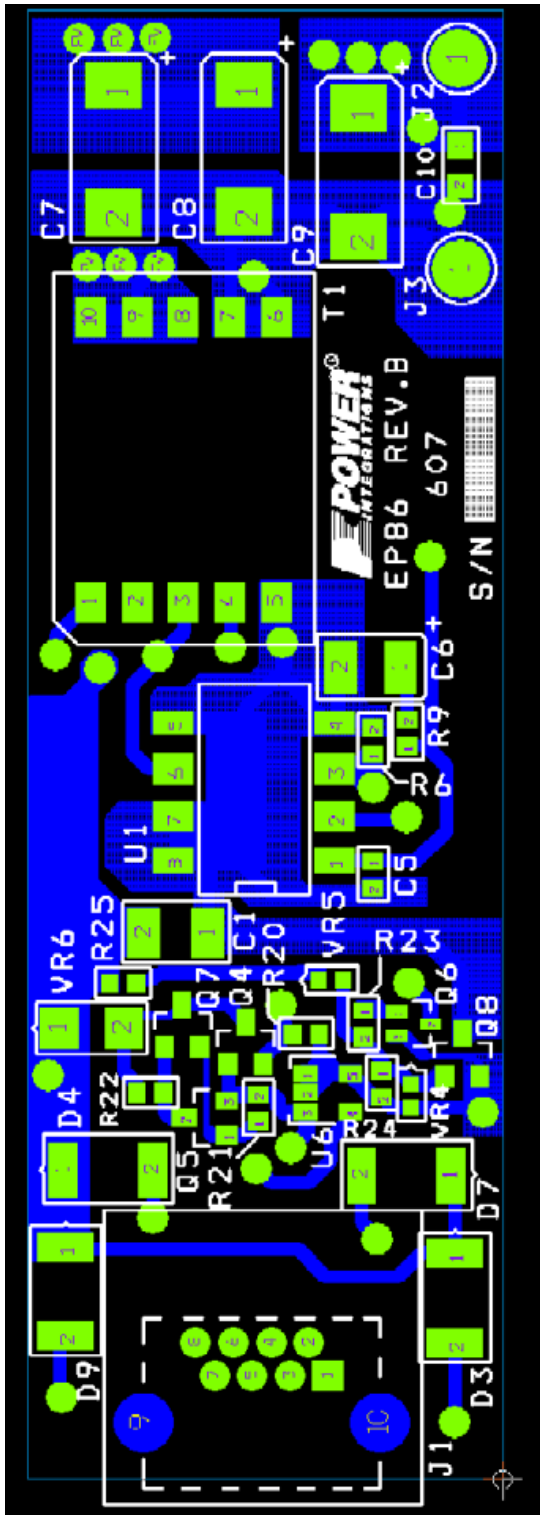

Figure 8 – PCB Layout Top Side.

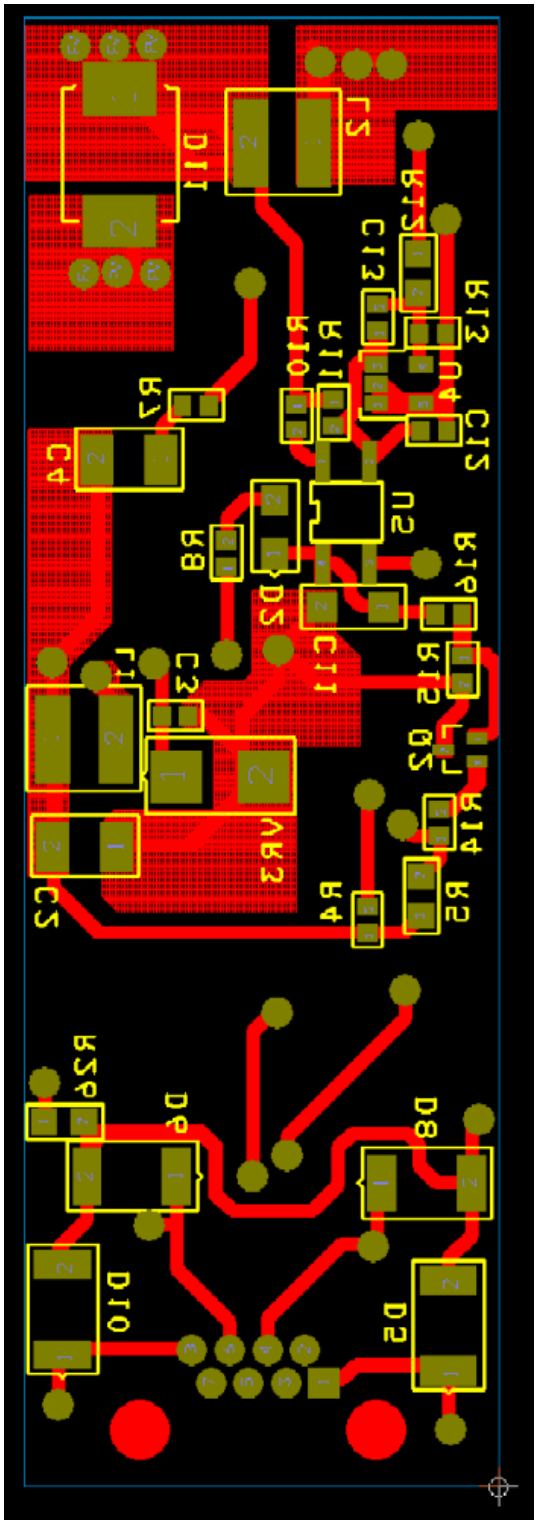

Figure 9 – PCB Layout Bottom Side.

7 Transformer Design Spreadsheet

DCDC_DPASwitch_Flyback_071405; Rev.2.7; Copyright Power Integrations 2005	INPUT	INFO	OUTPUT	UNITS	DPASwitch_Flyback_071405 - Continuous/Discontinuous mode Spreadsheet. Copyright 2005 Power Integrations
ENTER APPLICATION VARIABLES					**DC-DC Converter**
VDCMIN	36			Volts	Minimum DC Input Voltage
VDCMAX	57			Volts	Maximum DC Input Voltage
VO	3.3			Volts	Output Voltage (main)
PO	6.6	***Comment***		Watts	Verify temperature rise for continuous power. P and G packages may be thermally limited
n	0.8				Efficiency Estimate
Z			0.7		Loss Allocation Factor, (0.7 Recommended)
VB	14			Volts	Bias Voltage (Recommended between 12V and 18V)
UV AND OV PARAMETERS					
		min	max		
VUVOFF		30.0	33.1	Volts	Minimum undervoltage On-Off threshold
VUVON		32.2	34.7	Volts	Maximum undervoltage Off-On threshold (turn-on)
VOVON		74.9	-	Volts	Minimum overvoltage Off-On threshold
VOVOFF			94.7	Volts	Maximum overvoltage On-Off threshold (turn-off)
RL			619.0	k-Ohms	
ENTER DPASWITCH VARIABLES					
DPASWITCH	**DPA423G**			*16VDC*	*36 VDC*
Chosen Device	*DPA423G*		*Power Ou*	*6W*	*13W*
ILIMITMAX	*1.16*	*1.34*		Amps	From DPASWITCH Data Sheet
Frequency	**F**				Enter 'F' for fS = 400KHz and 'L' for fS = 300KHz
fS	*375000*			Hertz	DPASWITCH Switching Frequency
VOR	38		38	Volts	Reflected Output Voltage
KI	0.7		0.7		Current Limit Reduction Factor
ILIMITEXT			0.812	Amps	Minimum External Current limit
RX			11.0	k-Ohms	Resistor from X pin to source to set external current limit
VDS	1			Volts	DPASWITCH on-state Drain to Source Voltage
VD	0.5			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.7			Volts	Bias Winding Diode Forward Voltage Drop
KRP/KDP	0.62				Ripple to Peak Current Ratio (0.2 < KRP < 1.0 : 1.0< KDP<6.0)
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**ER14.5**				
Core Manuf					
Bobbin Manuf					
Core		*ER14.5*		*P/N:*	*ER14.5-3F3-S*
Bobbin		*ER14.5_Bobbin*		*P/N:*	*CPVS-ER14.5-1S-10P*
AE			0.176	cm^2	Core Effective Cross Sectional Area
LE			1.9	cm	Core Effective Path Length
AL			1400	nH/T^2	Ungapped Core Effective Inductance
BW			1.9	mm	Bobbin Physical Winding Width
M	0			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	2				Number of Primary Layers
NS	2				Number of Secondary Turns

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CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.52		Maximum Duty Cycle
IAVG			0.23	Amps	Average Primary Current
IP			0.64	Amps	Peak Primary Current
IR			0.40	Amps	Primary Ripple Current
IRMS			0.33	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			119	uHenries	Primary Inductance
NP			20		Primary Winding Number of Turns
NB			8		Bias Winding Number of Turns
ALG			297	nH/T^2	Gapped Core Effective Inductance
BP			2739	Gauss	Peak Flux density during transients (Limit to 3000 Gauss)
BM			2152	Gauss	Maximum Flux Density
BAC			667	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1203		Relative Permeability of Ungapped Core
LG			0.06	mm	Gap Length (Lg >> 0.051 mm)
BWE			3.8	mm	Effective Bobbin Width
TRANSFORMER SECONDARY DESIGN PARAMETERS					
ISP			6.38	Amps	Peak Secondary Current
ISRMS			3.15	Amps	Secondary RMS Current
IO			2.00	Amps	Power Supply Output Current
IRIPPLE			2.43	Amps	Output Capacitor RMS Ripple Current
VOLTAGE STRESS PARAMETERS					
VDRAIN			157	Volts	Maximum Drain Voltage (Includes Effect of Leakage Inductance)
PIVS			9	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB			36	Volts	Bias Rectifier Maximum Peak Inverse Voltage
ADDITIONAL OUTPUTS					
V_OUT2				Volts	2nd Output Voltage
VD_OUT2				Volts	2nd Output - Diode Forward voltage
N_OUT2			0.00		2nd Output - Turns
PIV_OUT2			0	Volts	2nd Output - Diode Peak Inverse Voltage
V_OUT3				Volts	3rd Output Voltage
VD_OUT3				Volts	3rd Output - Diode Forward voltage
N_OUT3			0.00		3rd Output - Turns
PIV_OUT3			0	Volts	3rd Output - Diode Peak Inverse Voltage
I_OUT2				Amps	2nd Output - Output Current
I_OUT3				Amps	3rd Output - Output Current
Negative Output			N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

8 Transformer Specification

8.1 Transformer Winding

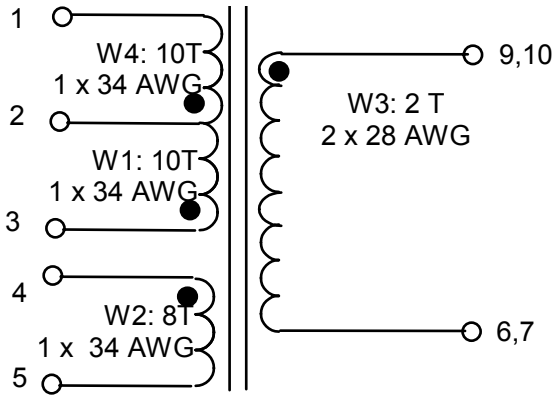

Figure 10 – Transformer Electrical Diagram.

8.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from Pins 1-5 to Pins 6-10	1500 VDC
Primary Inductance	Pins 1-3, all other windings open	120 μH, ±10%
Resonant Frequency	Pins 1-3, all other windings open	7.5 MHz (Min.)
Primary Leakage Inductance	Pins 1-3, with Pins 6/7-9/10 shorted	3.0 μH (Max.)

8.3 Materials

Item	Description
[1]	Core: ER14.5, Ferroxcube 3C96, 3F3 (or equivalent), A_{LG} = 312 nH/T^2
[2]	Bobbin: ER14.5, 10 pin
[3]	Magnet Wire: #34 AWG, Double Coated (Heavy Nyleze)
[4]	Magnet Wire: #28 AWG, Double Coated (Heavy Nyleze)
[5]	Tape: 3M 1298 Polyester Film (or equivalent), 1.8 mm wide
[6] (optional)	Core Clamp ER14.5 Ferroxcube CLM14.5
[7]	Varnish (DIPPED ONLY, NOT VACUUM IMPREGNATED)

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8.4 Transformer Build Diagram

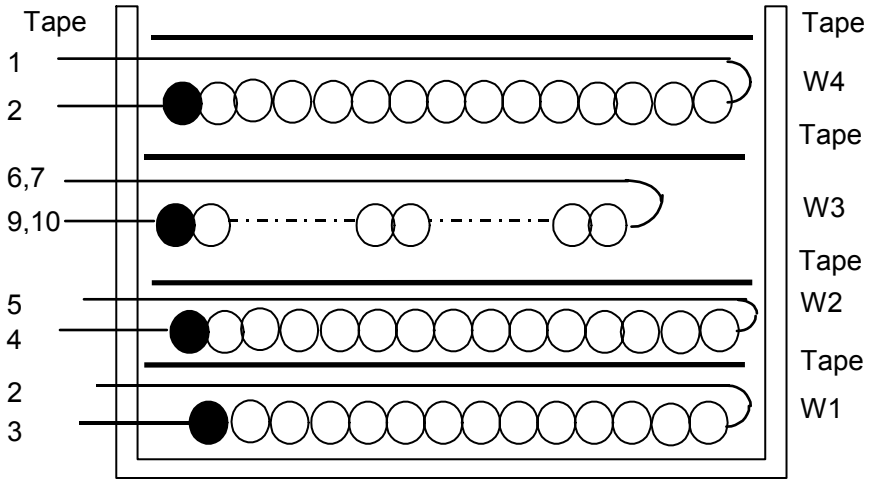

Figure 11 – Transformer Build Diagram.

8.5 Transformer Construction

Bobbin Preparation	Arrange bobbin & rotation such that primary start/finish wires do not overlap.
W1	Start at Pin 3. Wind 10 turns of item [3] in 1 layer. Bring finish lead back and terminate on Pin 2.
W2	Starting at Pin 4, wind 8 turns of item [3]. Spread turns evenly across bobbin in a single layer. Bring finish lead back and terminate on Pin 5.
Tape	Use one layer of item [5] for basic insulation.
W3	Start at Pins 9 and 10. Wind 2 turns of bifilar item [4] in 1 layer. Bring finish lead back and terminate on Pins 6 and 7.
Tape	Use one layer of item [5] for basic insulation.
W4	Continue from Pin 2. Wind 10 turns of item [3] in 1 layer. Bring finish lead back and terminate on Pin 1.
Outer Wrap	Use one layer of item [5] for basic insulation.
Final Assembly	Assemble and secure (glue or clamp, item [6]) core halves. Dip varnish item [7] and cure.

9 Performance Data

All measurements were taken at room temperature utilizing a DC input source and DC dynamic loads (except where resistive loads are specified). Input and output voltages and current were measured with dedicated digital multi-meters (DMMs).

9.1 Efficiency

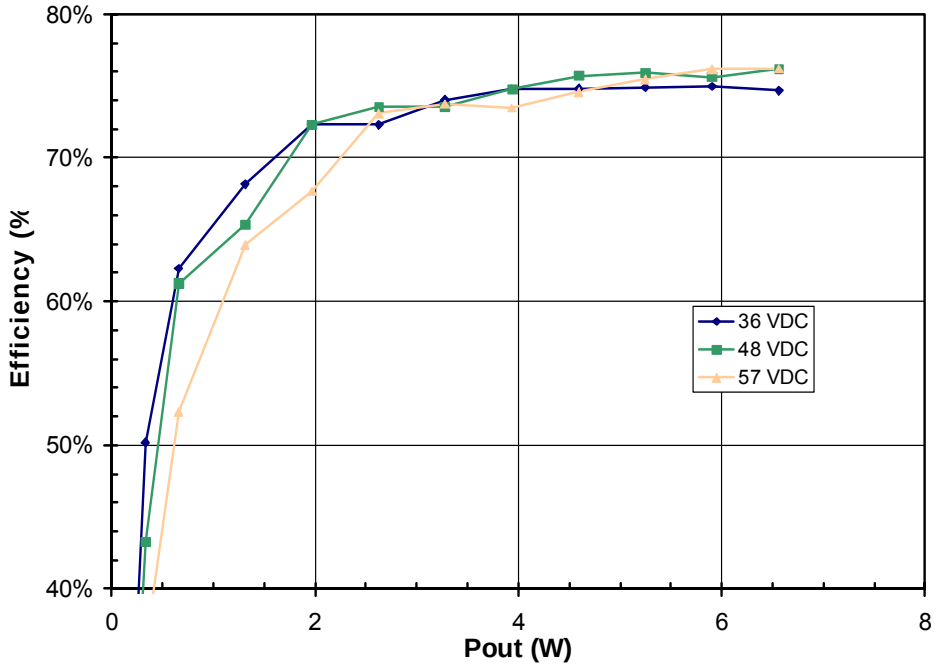

Figure 12 – Efficiency vs. Line and Load, Room Temperature.

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9.2 Load Regulation

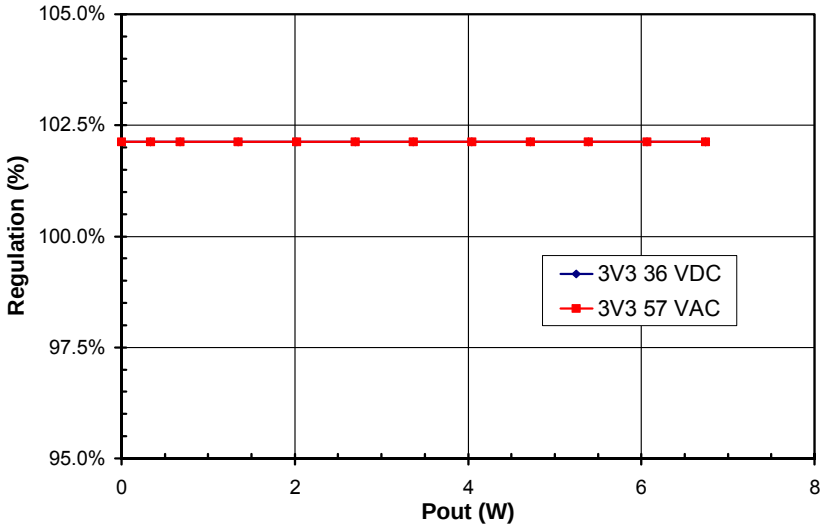

Figure 13 – Load Regulation, Room Temperature.

9.3 Line Regulation

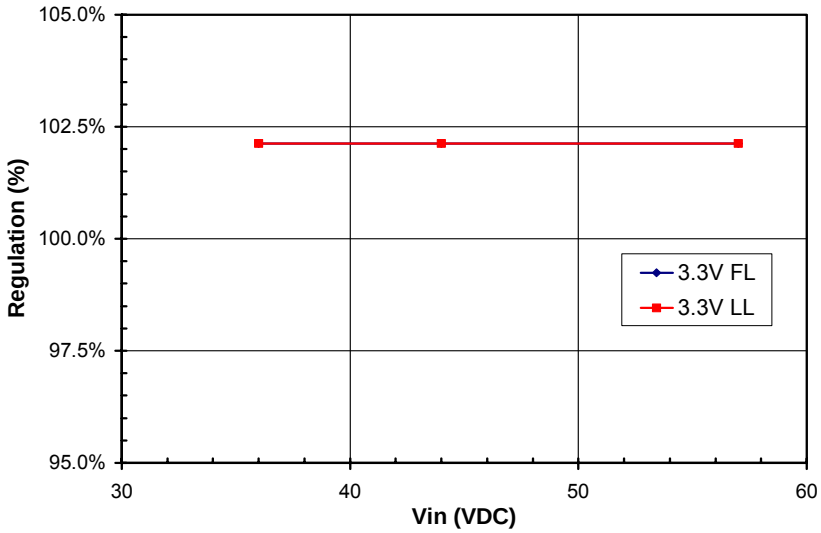

Figure 14 – Line Regulation, Room Temperature.

9.4 Overload Output Current

The DC output load current was recorded just prior to the auto-restart operation at various input line voltages. Performance was measured for various values of resistor R6.

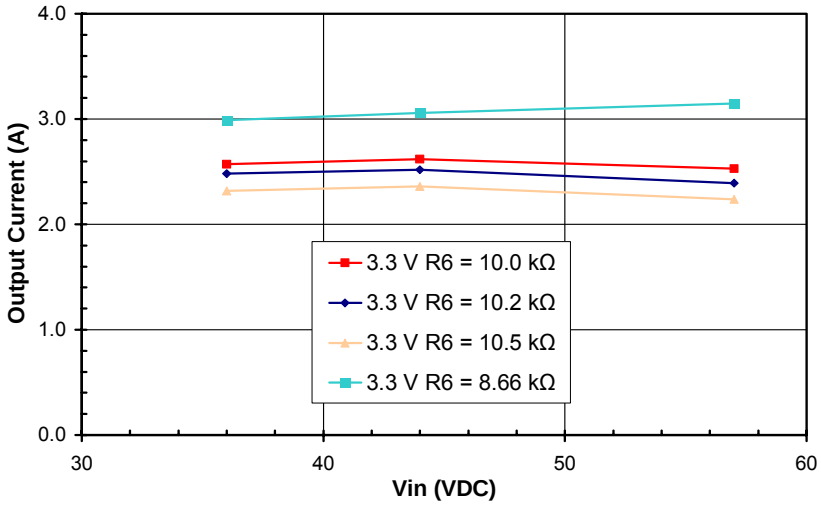

Figure 15 – Overload Output Current vs. Line Voltage for Different Values of R6, Room Temperature.

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10 Waveforms

10.1 Drain Voltage and Current, Full-Load Operation

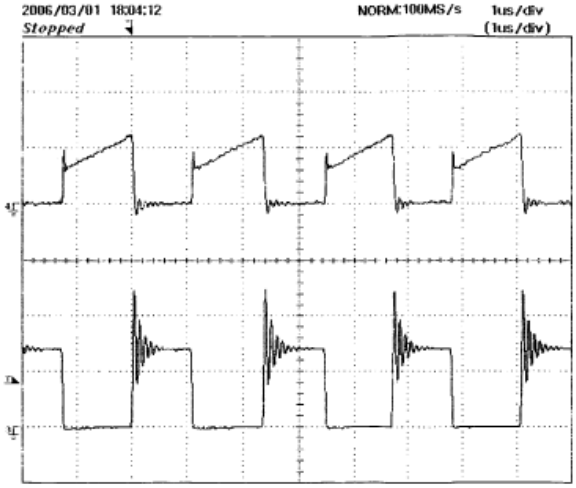

Figure 16 – 36 VDC, Full Load.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 50 V, 1 µs / div.

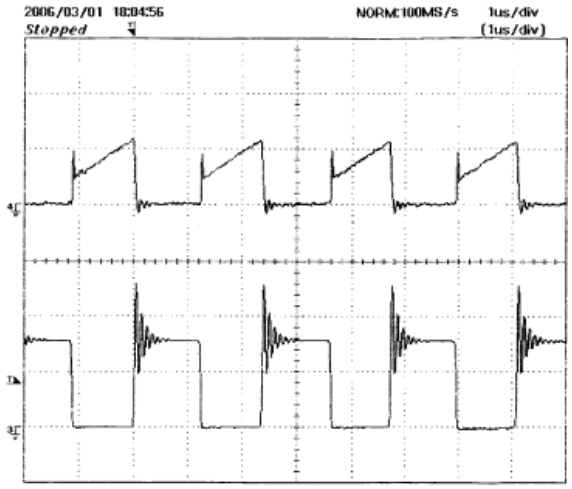

Figure 17 – 57 VDC, Full Load.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 50 V, 1 µs / div.

10.2 Output Voltage Start-Up Profile

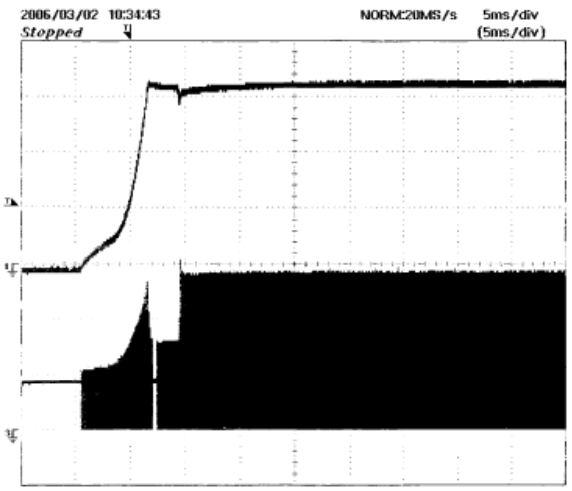

Figure 18 – Start-Up Profile, 36 VDC, No Load (worst-case).
Upper: V_{OUT}, 1 V / div.
Lower: V_{DRAIN}, 50 V, 1 µs / div.

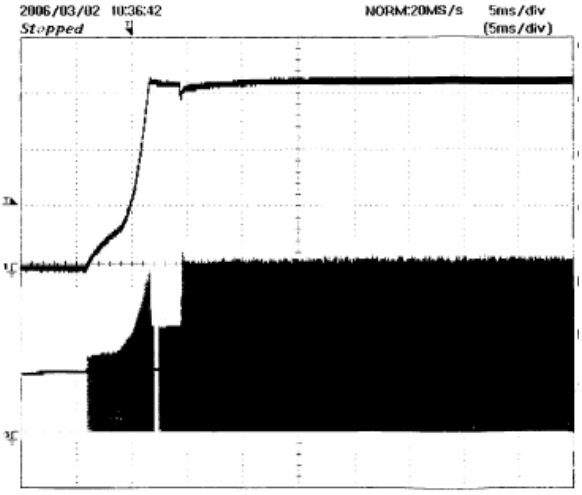

Figure 19 – Start-Up Profile, 57 VDC, No Load (worst-case).
Upper: V_{OUT}, 1 V / div.
Lower: V_{DRAIN}, 50 V, 1 µs / div.

10.3 Load Transient Response (75% to 100% Load Step)

In the figures shown below, signal averaging was used to better enable viewing of the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching is random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response.

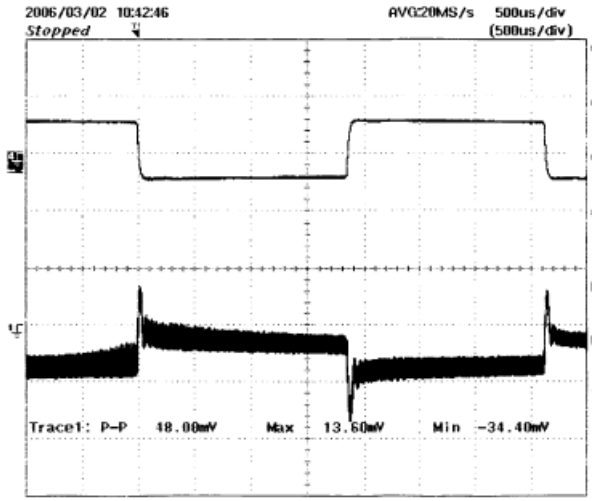

Figure 20 – Transient Response,
36 VDC, 75-100-75% Load Step.
Upper: Load Current, 1 A / div.
Lower: Output Voltage,
20 mV, 500 μs / div.

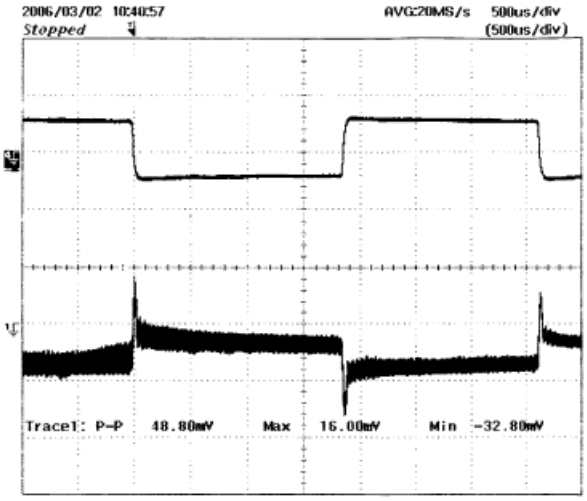

Figure 21 – Transient Response,
57 VDC, 75-100-75% Load Step.
Upper: Load Current, 1 A / div.
Lower: Output Voltage,
20 mV, 500 μs / div.

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10.4 Output Ripple Measurements

10.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signal pickup. Details of the probe modification are provided in Figures 22 and 23.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. ***Since the aluminum electrolytic type capacitor is polarized, proper polarity must be observed when connecting it to the output (see below).***

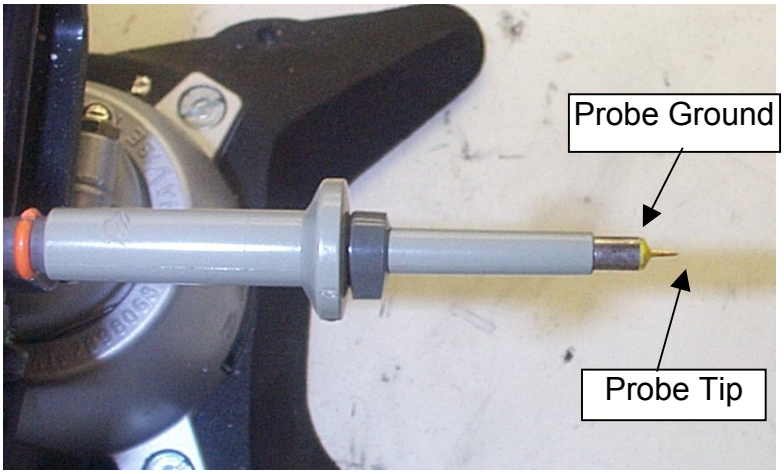

Figure 22 – Oscilloscope Probe Prepared for Ripple Measurement (End cap and ground lead removed).

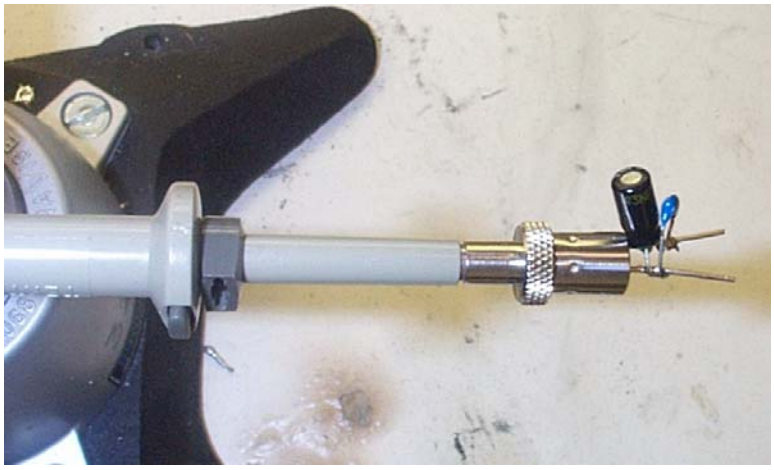

Figure 23 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added).

10.4.2 Output Ripple Measurements

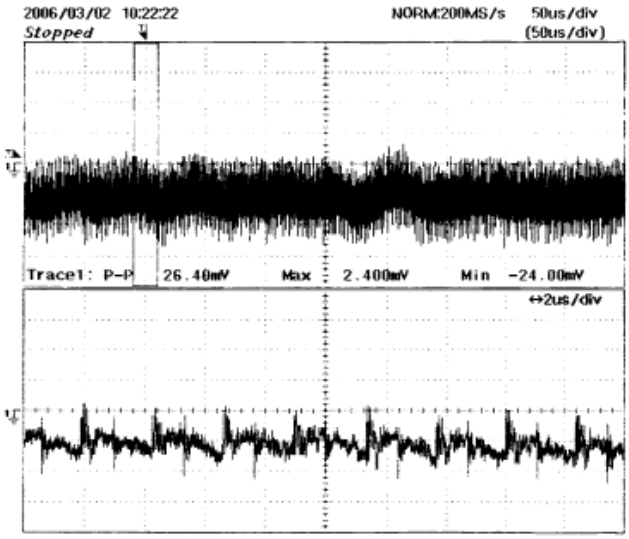

Figure 24 – Ripple, 36 VDC, Full Load.
Upper: 50 μs / div, 10 mV / div.
Lower: 2 μs / div, 10 mV / div.

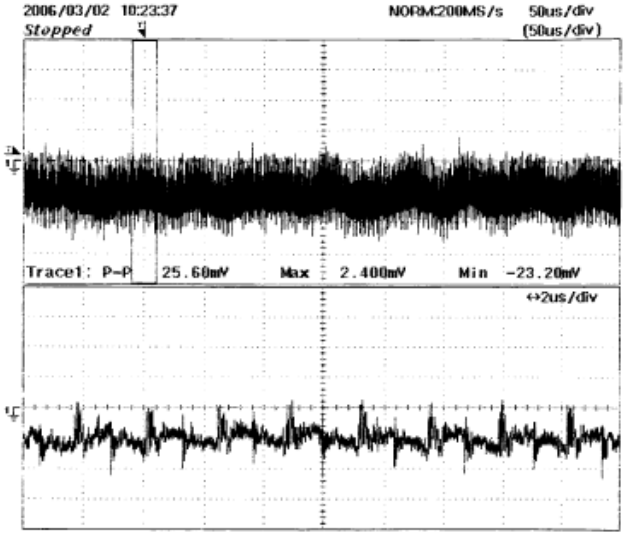

Figure 25 – Ripple, 48 VDC, Full Load.
Upper: 50 μs / div, 10 mV / div.
Lower: 2 μs / div, 10 mV / div.

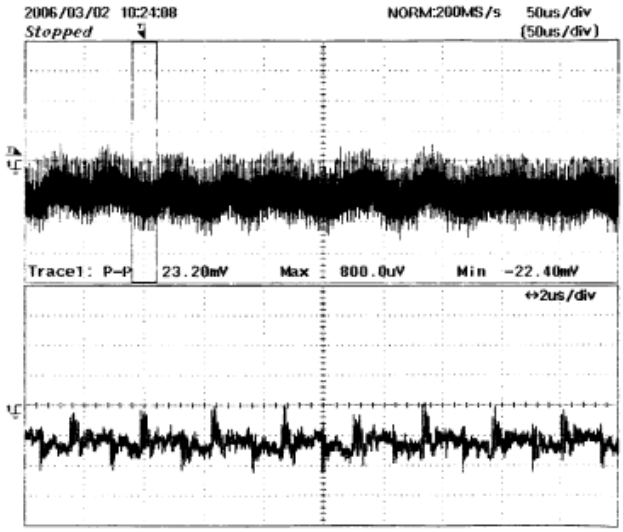

Figure 26 – Ripple, 57 VDC, Full Load.
Upper: 50 μs / div, 10 mV / div.
Lower: 2 μs / div, 10 mV / div.

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11 Revision History

Date	Author	Revision	Description & changes
January 3, 2006	RM/LN/ME	1.0	Initial release
April 13 2006	RM	1.1	Updated photo, layout, schematic and BOM

Notes

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WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@powerint.com

GERMANY
Rueckertstrasse 3
D-80336, Munich
Germany
Phone: +49-89-5527-3910
Fax: +49-89-5527-3920
e-mail: eurosales@powerint.com

JAPAN
Keihin Tatemono 1st Bldg
2-12-20
Shin-Yokohama, Kohoku-ku,
Yokohama-shi, Kanagawa ken,
Japan 222-0033
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

TAIWAN
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei, Taiwan 114, R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@powerint.com

CHINA (SHANGHAI)
Rm 807-808A,
Pacheer Commercial Centre,
555 Nanjing Rd. West
Shanghai, P.R.C. 200041
Phone: +86-21-6215-5548
Fax: +86-21-6215-2468
e-mail: chinasales@powerint.com

INDIA
261/A, Ground Floor
7th Main, 17th Cross,
Sadashivanagar
Bangalore, India 560080
Phone: +91-80-5113-8020
Fax: +91-80-5113-8023
e-mail: indiasales@powerint.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@powerint.com

EUROPE HQ
1st Floor, St. James's House
East Street, Farnham
Surrey, GU9 7TJ
United Kingdom
Phone: +44 (0) 1252-730-140
Fax: +44 (0) 1252-727-689
e-mail: eurosales@powerint.com

CHINA (SHENZHEN)
Room 2206-2207, Block A,
Elec. Sci. Tech. Bldg.
2070 Shennan Zhong Rd.
Shenzhen, Guangdong,
China, 518031
Phone: +86-755-8379-3243
Fax: +86-755-8379-5828
e-mail: chinasales@powerint.com

ITALY
Via Vittorio Veneto 12
20091 Bresso MI
Italy
Phone: +39-028-928-6000
Fax: +39-028-928-6009
e-mail: eurosales@powerint.com

SINGAPORE
51 Newton Road,
#15-08/10 Goldhill Plaza,
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@powerint.com

APPLICATIONS HOTLINE
World Wide +1-408-414-9660

APPLICATIONS FAX
World Wide +1-408-414-9760