

SY89850U

Precision Low-Power LVPECL Line Driver/Receiver with Internal Termination

General Description

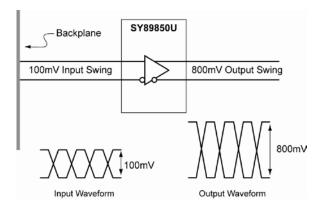
The SY89850U is a 2.5V/3.3V precision, high-speed, differential receiver capable of handling clocks up to 4GHz and data streams up to 3.2Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows users to interface to any differential signal (AC or DC-coupled) as small as 100mV ($200mV_{PP}$) without any level shifting or termination resistor networks in the signal path. The outputs are 800mV LVPECL, with extremely fast rise/fall times guaranteed to be less than 160ps.

The SY89850U operates from a 2.5V \pm 5% supply or a 3.3V \pm 10% supply and is guaranteed over the full industrial temperature range of -40°C to +85°C. The SY89850U is part of Micrel's high-speed, Precision Edge[®] product line.

All support documentation can be found on Micrel's web site at <u>www.micrel.com</u>.

Typical Application



Features

- Guaranteed AC performance over temperature and supply voltage:
 - DC- to > 3.2Gbps data rate throughput
 - 4GHz clock f_{MAX} (typ.)
 - <280ps In-to-Out t_{pd}
 - <160ps t_r/t_f
- Low power: 50mW (2.5V typ.)
- Ultra-low jitter design:
 - <1ps_{RMS} random jitter
 - <10ps_{PP} deterministic jitter
 - <10ps_{PP} total jitter (clock)
- Unique input termination and VT pin accepts DCand AC-coupled inputs (CML, PECL, LVDS)
- Typical 800mV (100k) LVPECL Output Swing
- Power supply 2.5V ±5% or 3.3V ±10%
- Industrial temperature range -40°C to +85°C
- Available in ultra-small (2mm x 2mm) 8-pin DFN package

Applications

- Backplane buffering
- OC-12 to OC-192 SONET/SDN clock/data distribution
- All Gigabit Ethernet clock or data distribution
- Fibre Channel distribution

Markets

- LAN/WAN
- Enterprise servers
- ATE
- Test and measurement

Precision Edge is a registered trademark of Micrel, Inc.



Ordering Information⁽¹⁾

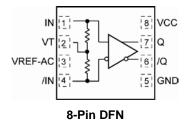
Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89850UMG	DFN-8	Industrial	850U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89850UMGTR ⁽²⁾	DFN-8	Industrial	850U with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for dice availability. Dice are guaranteed at $T_A = 25^{\circ}C$, DC Electrical Only.

2. Tape and Reel.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair is the signal to be buffered. These inputs accept AC- or DC-coupled signals as small as 100mV. Each pin of this pair internally terminates to a VT pin through 50Ω . Note that this input will default to an indeterminate state if left open. Please refer to the "Input Interface Applications" section for more details.
2	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to this pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details.
3	VREF-AC	Reference Output Voltage: This output biases to V _{CC} –1.2V. Connect to VT pin when AC-coupling the input. Bypass with 0.01µF low ESR capacitor to V _{CC} . Maximum sink/source current is ±1.5mA. Due to the limited drive capability, the VREF-AC pin is only intended to drive its respective VT pin. See "Input Interface Applications" section.
5	GND, Exposed Pad	Ground: Ground pin and exposed pad must be connected to the same ground plane.
7, 6	Q, /Q	Differential 100K LVPECL Output: This LVPECL output is the output of the device. Terminate through 50Ω to V _{CC} -2V. See "Output Interface Applications" section.
8	VCC	Positive Power Supply: Bypass with $0.1\mu F/\!/0.01\mu F$ low ESR capacitors as close to the VCC pin as possible.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V _{CC})	–0.5V to +4.0V
Input Voltage (V _{IN})	–0.5V to V _{CC}
LVPECL Output Current (I _{OUT})	
Continuous	
Surge	100mA
Input Current	
Source or sink current on IN, /IN	
Termination Current	
Source or sink current on VT	±100mA
Source or sink current on V _{REF-AC}	±2mA
Lead Temperature (soldering, 20sec.)	260°C
Storage Temperature (T _s)6	65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage (V _{CC})	. +2.375V to +2.625V
	+3.0V to +3.6V
Ambient Temperature (T _A)	–40°C to +85°C
Ambient Temperature (T _A) Package Thermal Resistance ⁽³⁾	
DFN (θ _{JA})	
Still-Áir	93°C/W
DFN (ψ _{JB})	
Junction-to-Board	60°C/W

DC Electrical Characteristics⁽⁴⁾

 $T_A = -40^{\circ}C$ to +85°C, unless noted.

Symbol	Parameter	Condition	Min	Тур	Max	Units
V _{cc}	Power Supply		2.375 3.0	2.5 3.3	2.625 3.6	V V
Icc	Power Supply Current	No load, max. V _{CC}		20	30	mA
$R_{\text{DIFF}_{IN}}$	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
R _{IN}	Input Resistance (IN-to-V _T), (/IN-to-V _T)		45	50	55	Ω
VIH	Input High Voltage (IN, /IN)	Note 5	V _{CC} -1.6		Vcc	V
VIL	Input Low Voltage (IN, /IN)		0		V _{IH} —0.1	V
V _{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a.	0.1		1.7	V
$V_{\text{DIFF}_\text{IN}}$	Differential Input Voltage Swing IN–/IN	See Figure 1b.	0.2			V
V_{T_IN}	In-to-V _T (IN, /IN)				1.28	V
V_{REF-AC}	Output Reference Voltage		V _{cc} -1.3	V _{cc} -1.2	V _{cc} -1.1	V

Notes:

1. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

3. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.

4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

5. V_{IH} (min) not lower than 1.2V.

LVPECL Output DC Electrical Characteristics⁽⁶⁾

 V_{CC} = +2.5V ±5% or +3.3V ±10%; T_A = -40°C to +85°C; R_L = 50 Ω to V_{CC} -2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Тур	Max	Units
V _{cc}	Output High Voltage Q, /Q		V _{CC} –1.145		V _{CC} -0.895	V
V _{OL}	Output Low Voltage Q, /Q		V _{CC} –1.945		V _{CC} -1.695	V
V _{OUT}	Output Voltage Swing Q, /Q	See Figure 1a.	550	800		mV
V _{DIFF_OUT}	Differential Output Voltage Swing Q, /Q	See Figure 1b.	1100	1600		mV

Note:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics⁽⁷⁾

 V_{CC} = +2.5V ±5% or +3.3V ±10%; T_A = -40°C to +85°C; R_L = 50 Ω to V_{CC} -2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Тур	Max	Units
f _{MAX}	Maximum Operating Frequency	NRZ Data	3.2			Gbps
		V _{OUT} ≥ 400mV Clock		4		GHz
t _{pd}	Propagation Delay IN-to-Q	V _{IN} ≥ 100mV	180	260	360	ps
t _{pd} Tempco	Differential Propagation Delay Temperature Coefficient			115		fs/°C
t _{JITTER}	Data Random Jitter (RJ)	Note 8			1	рs _{rms}
	Deterministic Jitter (DJ)	Note 9			10	PSPP
	Clock Cycle-to-Cycle Jitter	Note 10			1	ps _{RMS}
	Total Jitter (TJ)	Note 11			10	PS _{PP}
t _r , t _f	Rise/Fall Time (20% to 80%) Q, /Q	At full output swing.	50	100	160	ps

Notes:

7. The circuit is designed to meet the AC specifications shown in the above table after thermal equilibrium has been established.

8. Random jitter is measured with a K28.7 comma detect character pattern, measured at 2.5Gbps and 3.2Gbps.

9. Deterministic jitter is measured at 2.5Gbps and 3.2Gbps, with both K28.5 and 2²³–1 PRBS pattern.

10. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, T_n –T_{n-1} where T is the time between rising edges of the output signal.

11. Total jitter definition: with an ideal clock input of frequency < f_{MAX}, no more than one output edge in 10¹² output edges will deviate by more than the specified peak-to-peak jitter value.

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Single-Ended and Differential Swings

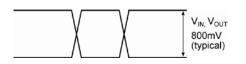
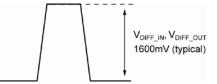
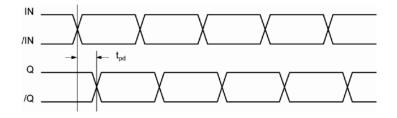


Figure 1a. Singled-Ended Voltage Swing



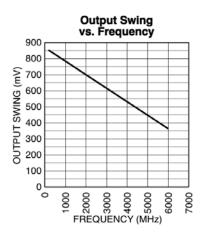


Timing Diagram



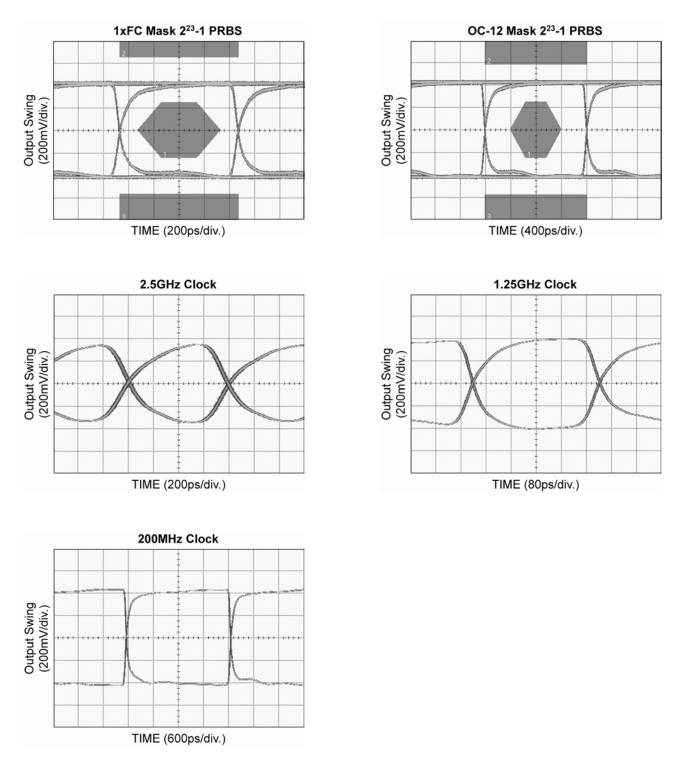
Typical Operating Characteristics

 $V_{CC}=3.3V,~GND=0V,~V_{IN}=\geq 400mV_{pp},~t_{r}/t_{f}\leq 300ps,~T_{A}=25^{\circ}C,~unless~otherwise~stated.$



Functional Characteristics

 $V_{CC} = 3.3V, \text{ GND} = 0V, V_{IN} = \ge 400 \text{mV}_{\text{pp}}, \text{t}_{\text{r}}/\text{t}_{\text{f}} \le 300 \text{ps}, \text{ T}_{\text{A}} = 25^{\circ}\text{C}, \text{ unless otherwise stated}.$



Input and Output Stages

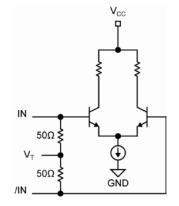


Figure 2a. Simplified Differential Input Stage

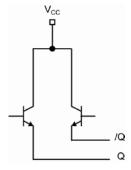
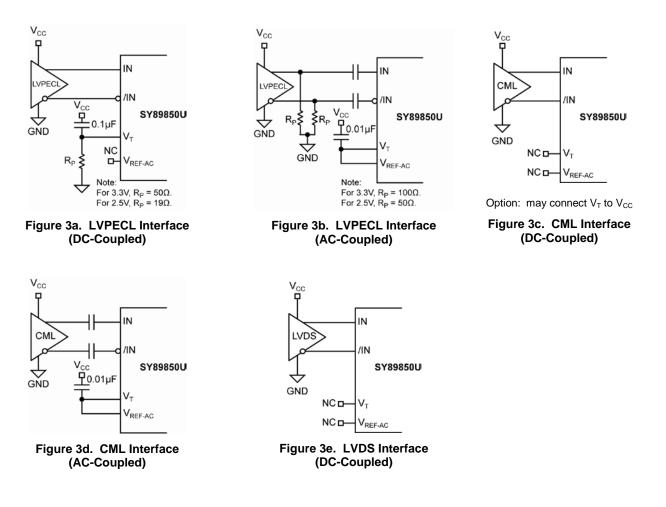


Figure 2b. Simplified LVPECL Output Stage

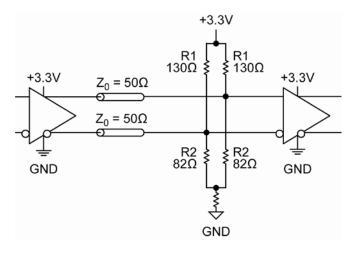
Input Interface Applications



Output Interface Applications

LVPECL has a high input impedance, a very low output impedance (open emitter), and a small signal swing which results in low EMI. LVPECL is ideal for driving \mathfrak{SD} - and $1\mathfrak{OD}$ -controlled impedance transmission lines. There are several techniques for

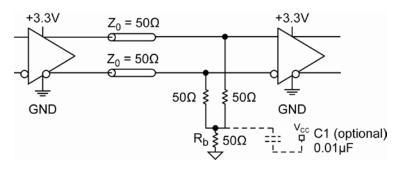
terminating the LVPECL output: Parallel Termination-Thevenin Equivalent, Parallel Termination (3-resistor), and AC-coupled Termination. Unused output pairs may be left floating. However, single-ended outputs must be terminated, or balanced.



Note:

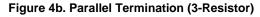
1. For +2.5V systems, $R1 = 250\Omega$, $R2 = 62.5\Omega$.





Notes:

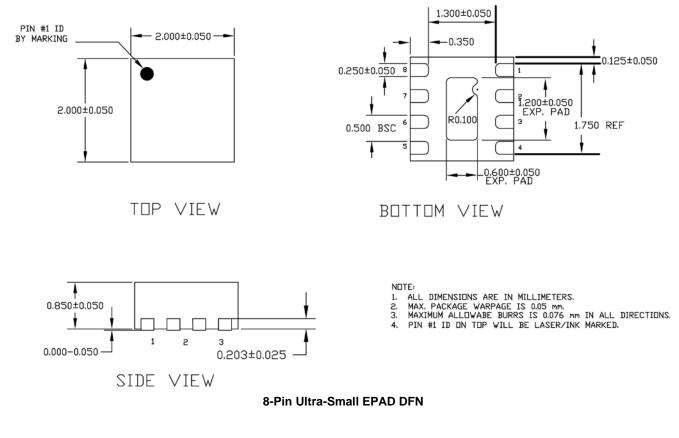
- 1. Power-saving alternative to Thevenin termination.
- 2. Place termination resistors as close to destination inputs as possible.
- 3. R_b resistor sets the DC bias voltage, equal to V_T .
- 4. For 2.5V systems, $R_b = 19\Omega$.



Related Product and Support Documentation

Part Number	Function	Data Sheet Link
SY58601U	Ultra-Precision Differential 800mV LVPECL Line Driver/Receiver with Internal Termination	www.micrel.com/product-info/products/sy58601u.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

Package Information



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